APPLICATION NOTE

- TDA6650/51TT -

3-BAND MIXER/OSCILLATOR AND LOW NOISE PLL
FOR DIGITAL AND TERRESTRIAL TUNERS

AN01014 _4

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Wide band AGC detector

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Purchase of Philips I^2C components conveys a license under the I^2C patent to use the components in the I^2C system, provided the system conforms to the I^2C specifications defined by Philips.

REVISION HISTORY

Version Number	Date	Change Description	Author
1.0	5/2/2001	Draft	J.BRILLANT / JM.PARIS
2.0	11/7/2002		J.BRILLANT
3.0	2/25/2004	➔ 3.3 Loop filter application for NTSC Japan & ISDB-T standards ➔ 4 wide band AGC	J.BRILLANT
4.0	2/25/2004	➔ 7 using a DC-DC converter	J.BRILLANT

CONTENTS

1 INTRODUCTION

The TDA6650/51TT is a programmable 3-band mixer/oscillator and low phase noise synthesizer, dedicated for hybrid (analog and digital) as well as pure digital terrestrial applications.

The IC is designed in a high-speed process with a fast phase detector to allow a high comparison frequency to reach the phase noise required for DVB-T applications.

The TDA6650/51TT is meant for use in analog and digital terrestrial tuning systems.

To operate and check the features of the TDA6650 and the TDA6651 2 demonstration boards were developed, they are described in this note.

2 TDA6650TT & TDA6651TT

2.1 GENERAL DESCRIPTION

The TDA6650/51TT is a programmable 3-band mixer/oscillator and low phase noise PLL synthesizer intended for pure 3-band tuner concepts applied to hybrid (digital and analog) terrestrial and cable TV reception.

The device includes three double balanced mixers for LOW, MID and HIGH bands and three oscillators for the corresponding bands, a switchable IF amplifier, a wide band AGC detector and a low noise PLL synthesizer. Two pins are available between the mixer output and the IF amplifier input to enable IF filtering for improved signal handling and to improve the adjacent channel rejection.

The IF amplifier is switchable in order to drive both symmetrical and asymmetrical outputs. When it is used as an asymmetrical amplifier, the IFOUTB pin needs to be connected to the supply voltage VCCA.

5 open drain PMOS are included on the IC, out of which 2 (BS1 and BS2) are also dedicated to the selection of the LOW, MID and HIGH bands. One of the PMOS ports (BS5) is coupled with the A/D converter.

The AGC detector provides information about the IF amplifier level. Six AGC take-over points are available by software. Two programmable AGC time constants are available for search tuning and normal tuner operation.

The Local Oscillator signal is fed to the fractional-N divider. The divided frequency is compared to the comparison frequency into the fast phase detector, which drives the charge-pump. The loop amplifier is also on-chip, including the high-voltage transistor to drive directly the 33 Volts tuning voltage without the need to add an external transistor.
The comparison frequency is obtained from an on-chip crystal oscillator. The crystal frequency can be output to the XTOUT pin to be used to drive the clock input of a digital demodulation IC.

Control data is entered via the I^2C-bus; six serial bytes are required to address the device, select the main divider ratio, the reference divider ratio, program the output ports, set the charge-pump current, enable or disable the crystal output buffer, select the AGC take-over point and time constant and/or select a specific test mode. Digital information concerning the AGC level detector and the ADC voltage can be read out of the TDA6650/51TT on the SDA line (one status byte) during a READ operation. A flag is set when the loop is “in-lock” and is read during a READ operation, as well as the Power-on reset flag and as the Automatic Loop Bandwidth Control flag. The device has 4 programmable addresses, programmed by applying a specific voltage to pin AS, enabling the use of multiple devices in the same system.

The I^2C bus is fast mode compatible and is compatible with 5V, 3.3V and 2.5V micro-controllers depending on the voltage applied on pin BVS.

2.2 APPLICATION AREAS

- Analog and digital terrestrial tuning systems (OFDM, PAL...).
- Digital Set-top boxes.
- Cable tuners (QAM).
- Digital TV sets.

2.3 FEATURES

- Single-chip 5V mixer/oscillator and low phase noise PLL synthesizer for TV and VCR tuners, dedicated to hybrid (analog and digital) as well as pure digital terrestrial applications.
- 5 possible step frequencies to cope with different digital terrestrial TV standards and with analog TV.
- 8 charge-pump currents between 38μA and 580μA to reach the optimum phase noise performance over the bands.
- Automatic Loop Bandwidth Control (ALBC) sets the optimum phase noise performance for all channels (see paragraph 3.4.ALBC in TDA6650/51TT).
- I²C-bus protocol compatible with 2.5 V, 3.3 V and 5 V micro-controllers:
  - Address + 4 data bytes transmission (I²C-bus 'write' mode).
  - Address + 1 status byte (I²C-bus 'read' mode).
  - 4 independent I²C-bus addresses.
- 5 PMOS open drain ports with 15mA source capability for band-switching and general purpose. One of these ports is combined with the 5-steps A/D converter.
- Wide band AGC detector for internal tuner AGC:
  - 6 programmable take-over points.
  - 2 programmable time constants.
  - AGC flag.
- In-lock flag.
- Crystal frequency buffer output.
- 33 V tuning voltage output.
- 15-bit programmable divider.
- Varicap drive disable.
- Balanced mixers with a common emitter input for the LOW band and for MID band (each single input).
- Balanced mixer with a common base input for HIGH band (balanced input).
- 2-pin asymmetrical oscillators for the LOW band and the MID band.
- 4-pin symmetrical oscillator for HIGH band.
- Switched concept IF amplifier with both asymmetrical and symmetrical outputs.

2.4 BLOCK DIAGRAM

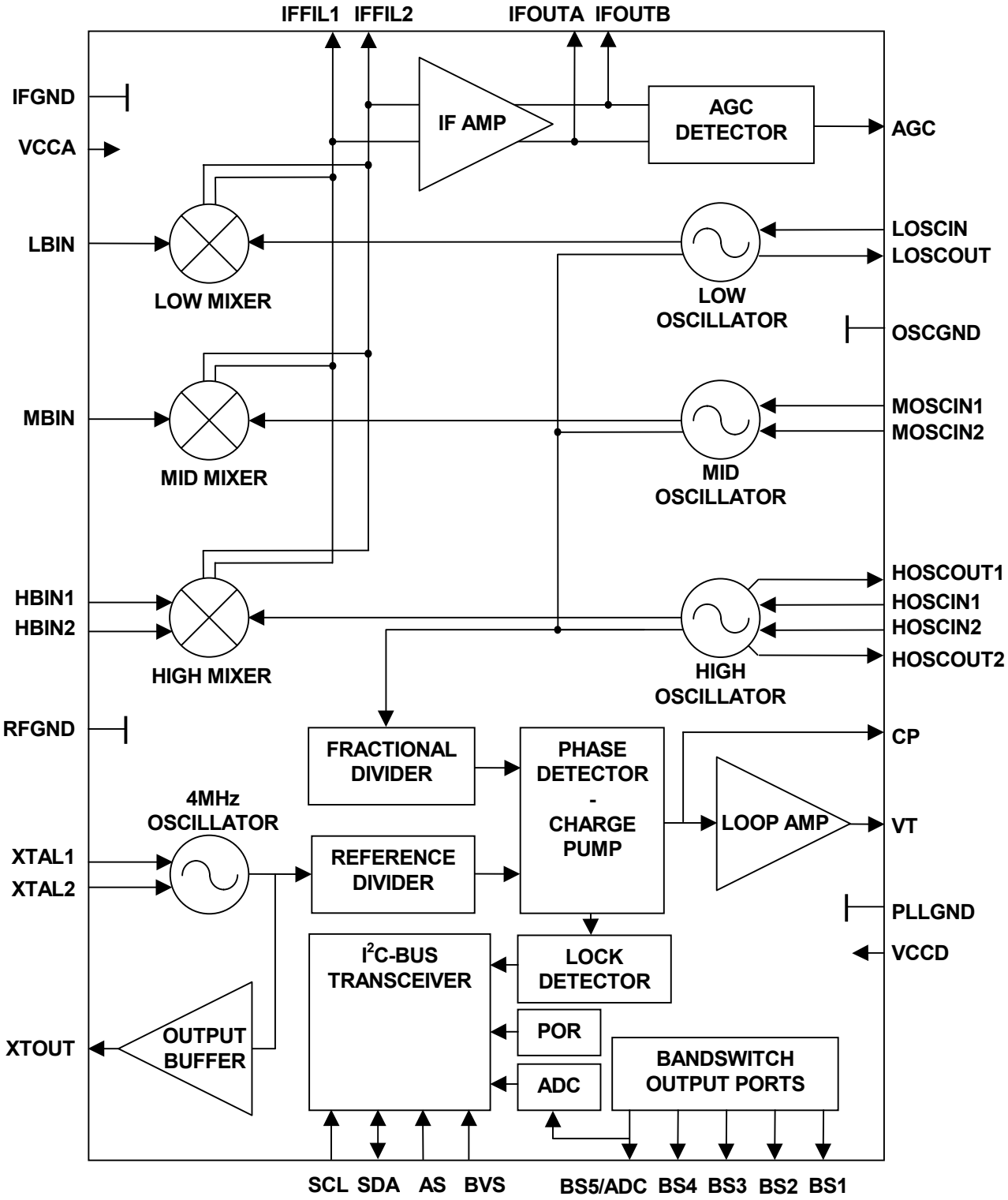


figure 1. Block diagram.

2.5 PIN ASSIGNMENT

2.5.1 Pinning

SYMBOL	PIN		DESCRIPTION
	6650	6651	
HBIN1	1	38	HIGH band RF input
HBIN2	2	37	HIGH band RF input
MBIN	3	36	MID band RF input
LBIN	4	35	LOW band RF input
RFGND	5	34	RF ground
IFFIL1	6	33	IF filter output
IFFIL2	7	32	IF filter output
BS4	8	31	PMOS open drain output port for general purpose
AGC	9	30	AGC output
BS3	10	29	PMOS open drain output port for general purpose
BS2	11	28	PMOS open drain output port to select the MID band
BS1	12	27	PMOS open drain output port to select the LOW band
BVS	13	26	Bus voltage selection input
ADC/BS5	14	25	PMOS open drain output port for general purpose / ADC input
SCL	15	24	I^2C bus serial clock input
SDA	16	23	I^2C bus serial data input / output
AS	17	22	I^2C bus address selection input
XTOUT	18	21	Crystal frequency buffer output
XTAL1	19	20	Crystal oscillator input
XTAL2	20	19	Crystal oscillator input
N.C	21	18	Not connected
VT	22	17	Tuning voltage output
CP	23	16	Charge pump output
VCCD	24	15	Supply voltage for the PLL part
PLLGND	25	14	PLL ground
VCCA	26	13	Supply voltage for the analog part
IFOUTB	27	12	IF amplifier output for symmetrical amplifier and asymmetrical IF amplifier switch input
IFOUTA	28	11	IF amplifier output
IFGND	29	10	IF ground
HOSCIN1	30	9	HIGH band oscillator input
HOSCOUT1	31	8	HIGH band oscillator output
HOSCOUT2	32	7	HIGH band oscillator output
HOSCIN2	33	6	HIGH band oscillator input
MOSCIN1	34	5	MID band oscillator input
MOSCIN2	35	4	MID band oscillator output
OSCGND	36	3	Oscillator ground
LOSCOUT	37	2	LOW band oscillator output
LOSCIN	38	1	LOW band oscillator input

Table 1. TDA6650TT & TDA6651TT pinning.

2.5.2 Pin configuration

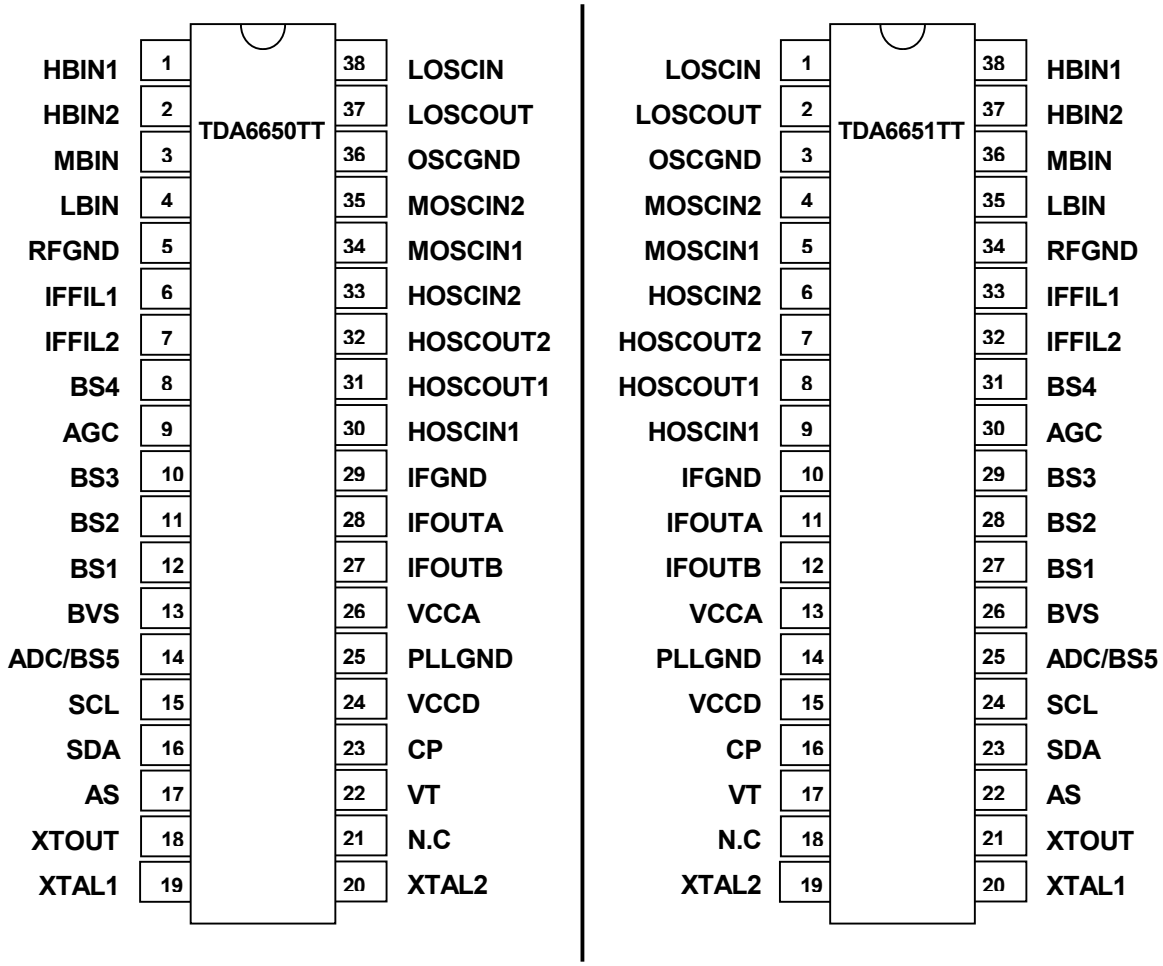


figure 2. Pin configuration.

3 LOOP FILTER DESIGN

3.1 Principle

All applications using a Voltage Controlled Oscillator (VCO) and a Phase Locked Loop (PLL) can be modeled as a second order loop system. That system may be characterized with its closed loop transfer but also with its open loop transfer. The study of the open loop transfer (G_{OL}) guaranties the loop stability; and the closed loop transfer gives information on phase noise performances. Three parameters will be used to optimize the design of that loop: phase margin, peaking and closed loop bandwidth.

3.1.1 Open loop transfer function

Calculations show that the open loop transfer function G_{OL} is:

(equation 1.)

$$G_{OL}(jw) = \frac{I_{cp}.K_{vco}}{\left(\frac{f_{VCO}}{f_{comp}}\right).C_1} \cdot \frac{(1 + j.R_2.C_1.w)}{w^2.(1 + j.R_2.C_2.w).(1 + j.R_p.C_p.w)}$$

With:
- I_{cp} charge pump current (A),
- K_{vco} local oscillator slope (Hz/V),
- f_{VCO} VCO frequency (Hz),
- f_{comp} comparison frequency (Hz) (related to the frequency step, see Table 2)
- R_2, R_p, C_1, C_2 and C_p are the components the loop filter (see figure 3).
-

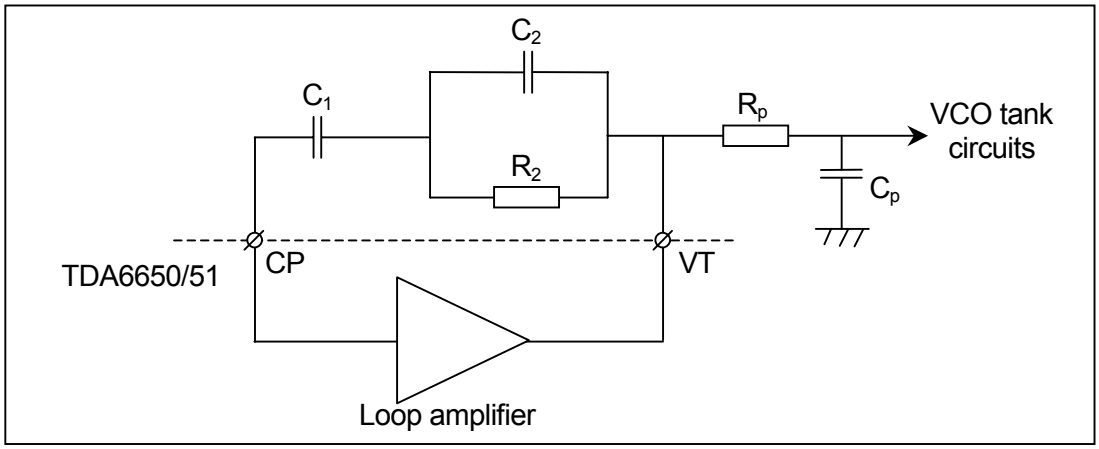


figure 3. Components of the loop filter and the post filter

NB: the comparison frequency, f_{comp}, is not equal to the step frequency in the TDA6650/51. This is due to the fractional-N architecture used (see paragraph 6.principle of the low noise PLL).

step frequency	comparison frequency
50kHz	1MHz
62.5kHz	2MHz
125kHz	4MHz
142.86kHz	4MHz
166.67kHz	4MHz

Table 2. Relation between f_{comp} and the step frequency in the TDA6650/51.

When studying magnitude and phase of open loop transfer, we define the phase margin of the system (see figure 4):

(equation 2.) $$PHASE\ MARGIN = phase\ of\ open\ loop\ transfer + 180°$$

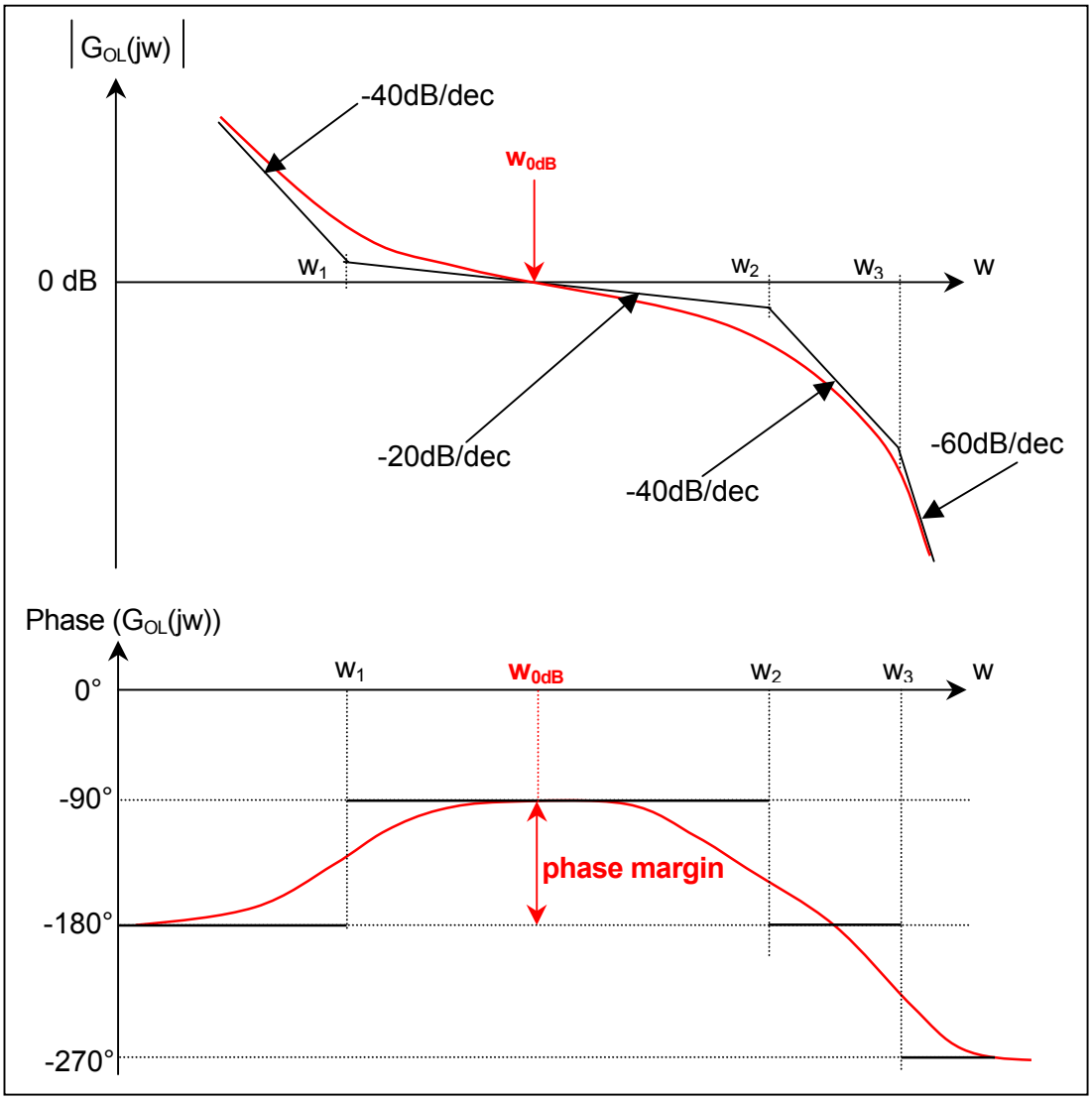


figure 4. magnitude and phase of open loop transfer

NB: $w_1 = \frac{1}{R_2.C_1}$, $w_2 = \frac{1}{R_2.C_2}$ and $w_3 = \frac{1}{R_p.C_p}$

The stability of the loop may be guaranteed if that phase margin is high enough (at least higher than 30°). Otherwise the loop may become unstable depending on the various spreads (loop filter components, PLL and VCO parameters…).

3.1.2 Closed loop transfer function

The closed loop transfer function G_{CL} is obtained from the open loop transfer function:

(equation 3.)

$$G_{CL}(jw) = \left(\frac{f_{VCO}}{f_{comp}}\right).\frac{G_{OL}(jw)}{1+G_{OL}(jw)}$$

When studying magnitude of that closed loop transfer function, we define the “peaking” and the closed loop bandwidth.

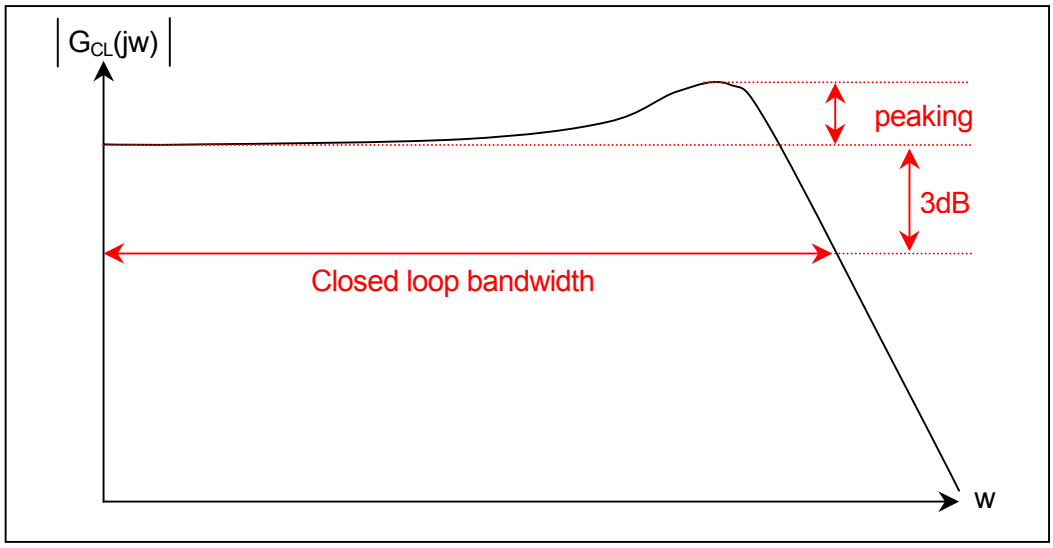


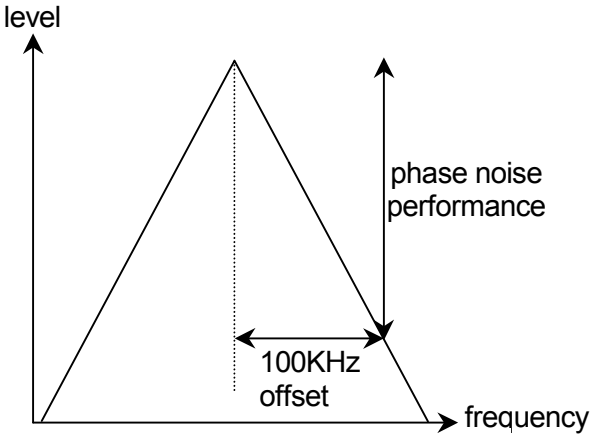
figure 5. magnitude of closed loop transfer

The closed loop bandwidth is usually called PLL bandwidth.

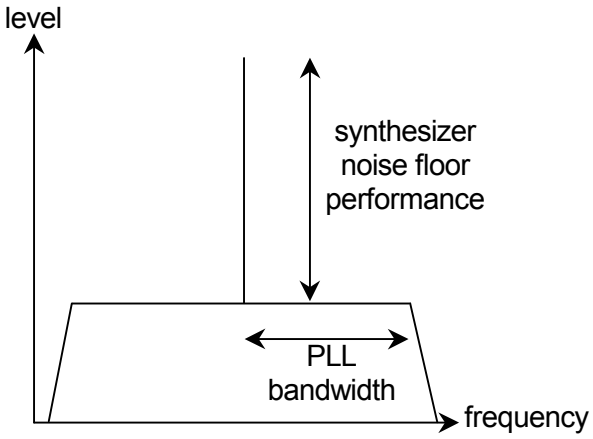
The “peaking” effect is linked to the phase margin: if the phase margin is high (close to 90°) the ”peaking” is low (close to 0dB). When a peaking effect is visible on closed loop transfer function, phase noise increases around the peaking frequency.

3.1.3 Influence of the loop filter design on phase noise performance

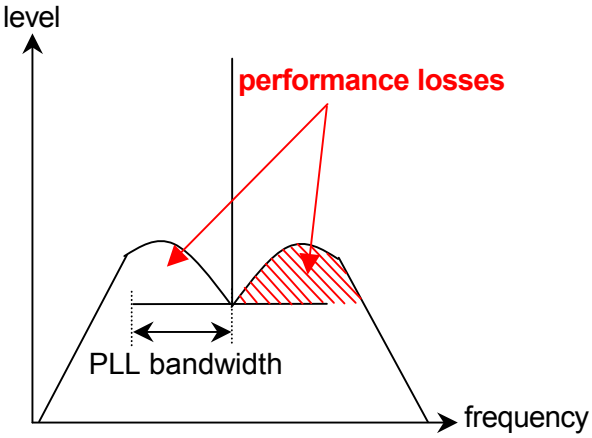
The loop filter might be adapted in order to satisfy two requests: loop stability (phase margin and peaking) and phase noise matching between PLL and VCO. The loop filter determines the PLL bandwidth, that bandwidth has to fit with VCO phase noise performances, practical considerations are expressed on the figure 6.



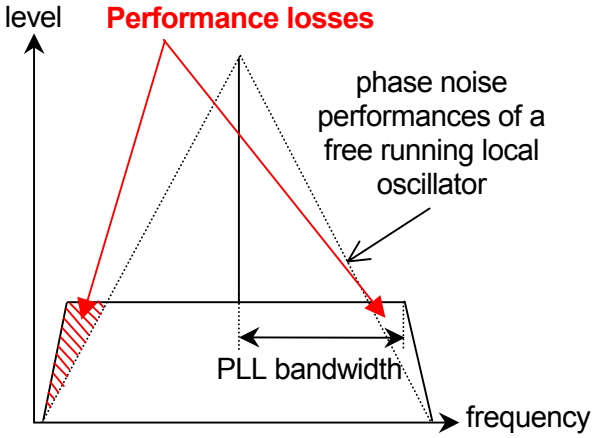
phase noise characteristics of a free running local oscillator



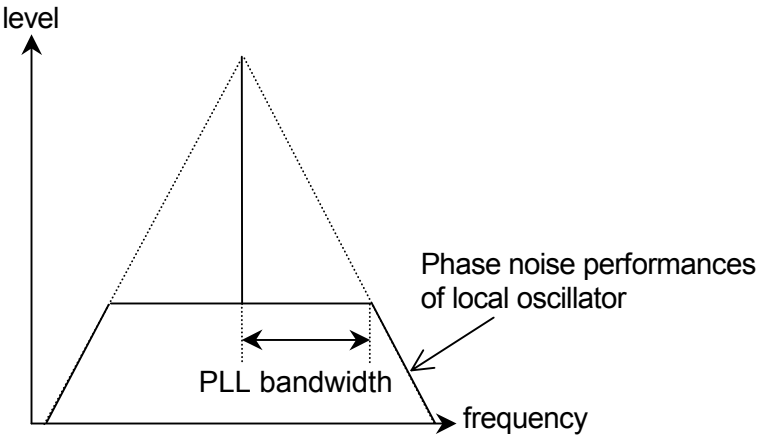
PLL characteristics



Case 1: PLL bandwidth is too narrow



Case 2: PLL bandwidth is too large



Case 3: matching between PLL bandwidth and phase noise performances

figure 6. matched and unmatched applications

3.1.4 Introduction of the integrated jitter function

3.1.4.1 Definition of the integrated phase jitter:

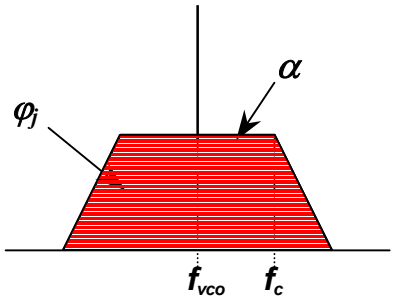
When an integrated circuit is dedicated to the digital reception tuning systems, no longer the phase-noise as it was specified on analog reception tuning systems is used. The so-called integrated phase jitter (φ_j) becomes the parameter needed for qualifying the PLL/VCO phase-noise performance.
The application of the demonstration board has been optimized using the integrated jitter measurement result.

By total integration calculations based on a Gaussian spectral noise density law, it can be shown that in a phase locked oscillator, the residual integrated jitter is defined as follow: (based on the hypothesis that the PLL bandwidth fits exactly with the phase-noise of the oscillator)

$$\varphi_j(\text{deg}) = \frac{360}{\pi}.\sqrt{f_C.10^{\frac{\alpha}{10}}}$$

or

$$\varphi_j(rad) = 2.\sqrt{f_C.10^{\frac{\alpha}{10}}}$$



where f_c is the bandwidth (Hz) of the PLL, and α the phase-noise (dBc/√Hz) at the frequency offsets $f < f_c$.

When the PLL bandwidth does not fit with the slope of the VCO phase-noise, the formula (see above) is not applicable anymore, and only the measurement allows the quantification of φ_j by a simple way.

3.1.4.2 Measurement method:

The measurements were performed with and ROHDE & SCHWARZ FSEA Spectrum-Analyzer with the built-in FSE-K4 software. This software allows a monitoring the phase-noise curve and the result of integrated jitter (called residual PM). An example of integrated jitter measurement is given below (see figure 7).

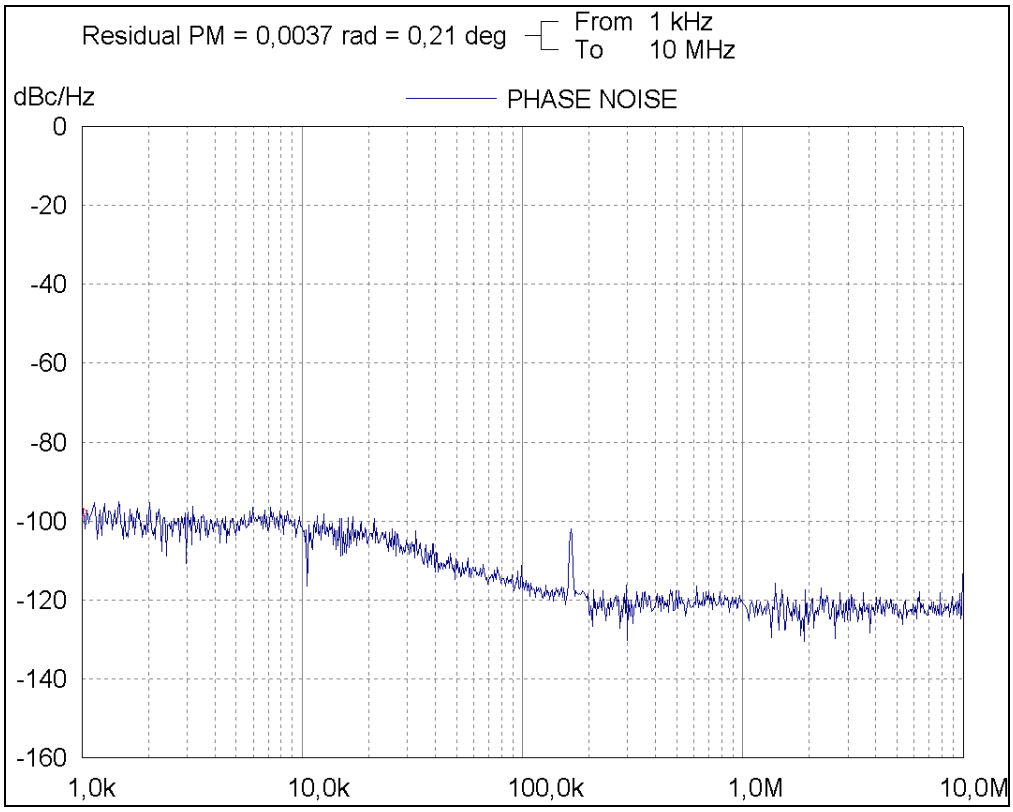


figure 7. Integrated phase jitter measurement on the demonstration board (VCO frequency of 80.1667MHz, frequency step 166.67kHz)

3.2 Loop filter application for PAL & DVB-T standards

Three applications are described in this chapter, all dedicated to the European market: one is dedicated to digital reception only (DVB-T), two other intend to address hybrid reception (PAL & DVB-T). The figures included in this report are given as typical values. The proposed applications (the pure digital application and the conventional hybrid application) have been used for the IC qualification.

● **Validity domain**

The present chapter is dedicated to the European standards (PAL & DVB-T standards). All measurements and simulations were performed with local oscillators tuned with respect to the TDA6650/51 specification.

	RF inputs		oscillators	
	min	max	min	max
low	44,25	157,25	83,15	196,15
mid	157,25	443,25	196,15	482,15
high	443,25	863,25	482,15	902,15

Table 3. Local oscillators frequency coverage.

If the oscillators are tuned with different ranges, the measurement results may change (some other optimizations can be necessary).

The IF intermediate frequency programmed for the measurements is:
- 36.1667MHz DVB-T application.
- 38.9MHz PAL application.

3.2.1 Pure digital application (DVB-T standard)

● **Specification points**

Two main parameters are used to design the MOPLL application:
- The phase noise performance.
- The step frequency spurious rejection.

The minimum performances are:
- Phase noise @1kHz < –82dBc/Hz.
- Phase noise @10kHz < –87dBc/Hz.
- Phase noise @100kHz < –104dBc/Hz.
- Frequency step spurious < –50dBc. (relative to the carrier)

● **Digital application - software programming**

A loop filter application in association with a charge-pump table determines the PLL loop characteristics. First of all, the loop filter should guaranty the system stability (phase margin), then, it has to fulfil the appropriate PLL bandwidth to reach the required spurious rejection and also to allow a low synthesizer noise floor:

1. The loop stability is obtained provided the phase margin of the PLL second order loop is high enough. All the filters presented in this chapter ensure a phase margin of 40° (worst case).
2. The phase noise performances are reached by designing a loop filter that adjusts the PLL bandwidth (see figure 6).

Note: for every application a single optimized charge-pump table can be simulated.

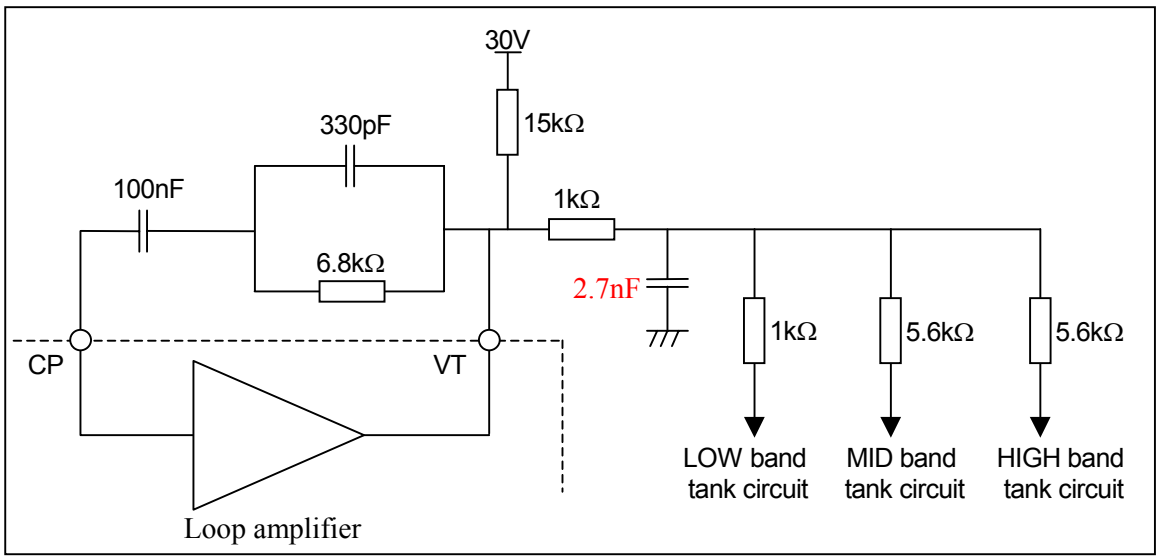


figure 8. Loop filter for pure digital application (DVB-T standard).

The TDA6650/51 is able to synthesize a Local Oscillator frequency with 5 different steps. In the fractional architecture those 5 different steps corresponds to 3 comparison frequencies. The loop filter design is only affected by the comparison frequency; therefore a charge-pump current table is linked to the comparison frequency in use. The table below is dedicated to the digital reception therefore to the 4MHz comparison frequency (frequency step 125kHz, 142.86kHz and 166.67kHz).

band	osc (MHz)	RF (MHz)	charge pump current (uA)
	80 to 92	44 to 56	60
	92 to 144	56 to 108	90
	144 to 156	108 to 120	130
	156 to 176	120 to 140	190
	176 to 184	140 to 148	280
LOW	184 to 193	148 to 157	410
	196 to 224	160 to 188	60
	224 to 296	188 to 260	90
	296 to 380	260 to 344	130
	380 to 404	344 to 368	190
	404 to 448	368 to 412	280
	448 to 472	412 to 436	410
MID	472 to 479	436 to 443	600
	484 to 604	448 to 568	130
	604 to 676	568 to 640	190
	676 to 752	640 to 716	280
	752 to 868	716 to 832	410
HIGH	868 to 900	832 to 864	600

Table 4. Charge-pump current programming for the 4MHz comparison frequency in the digital application (DVB-T standard) (corresponding to the ALBC feature).

All the measurements described in this paper where performed on the TDA6651 demonstration board (PCB 827-3).

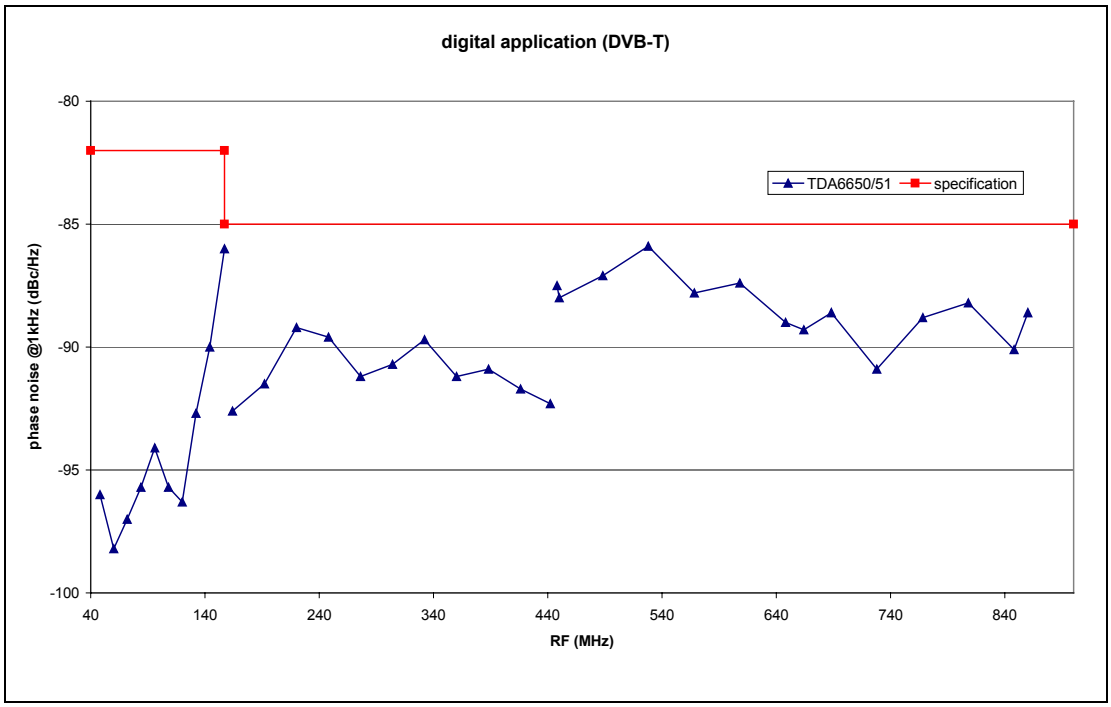


figure 9. 1kHz - phase noise measurement in the digital application (DVB-T).

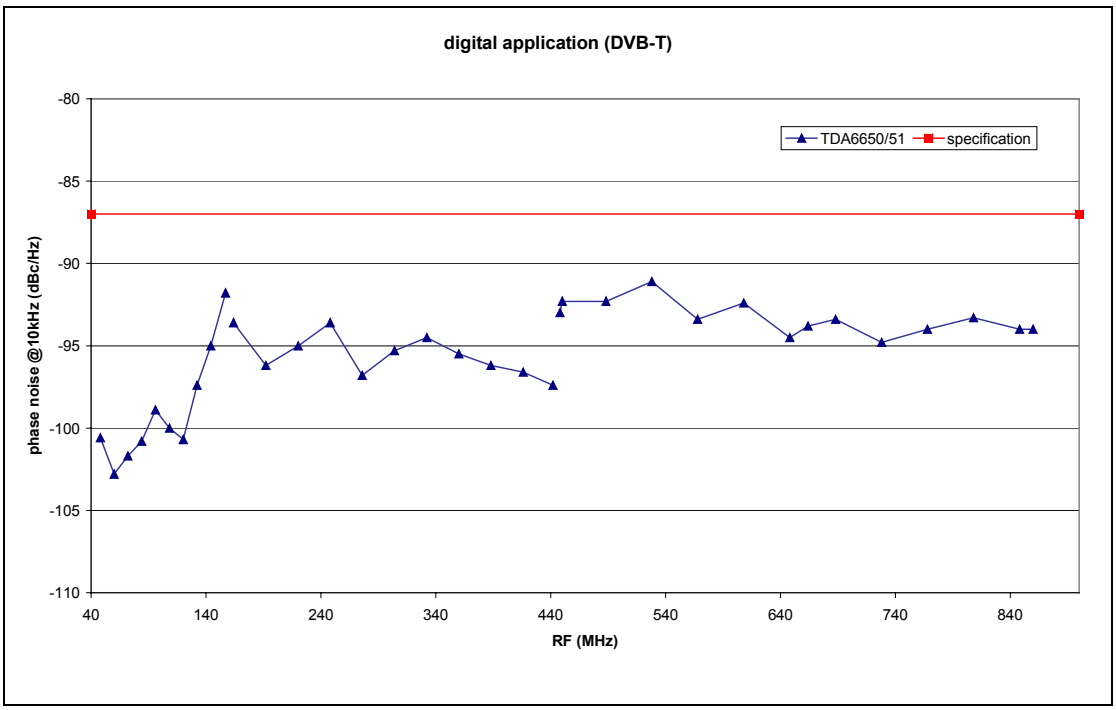


figure 10. 10kHz - phase noise measurement in the digital application (DVB-T).

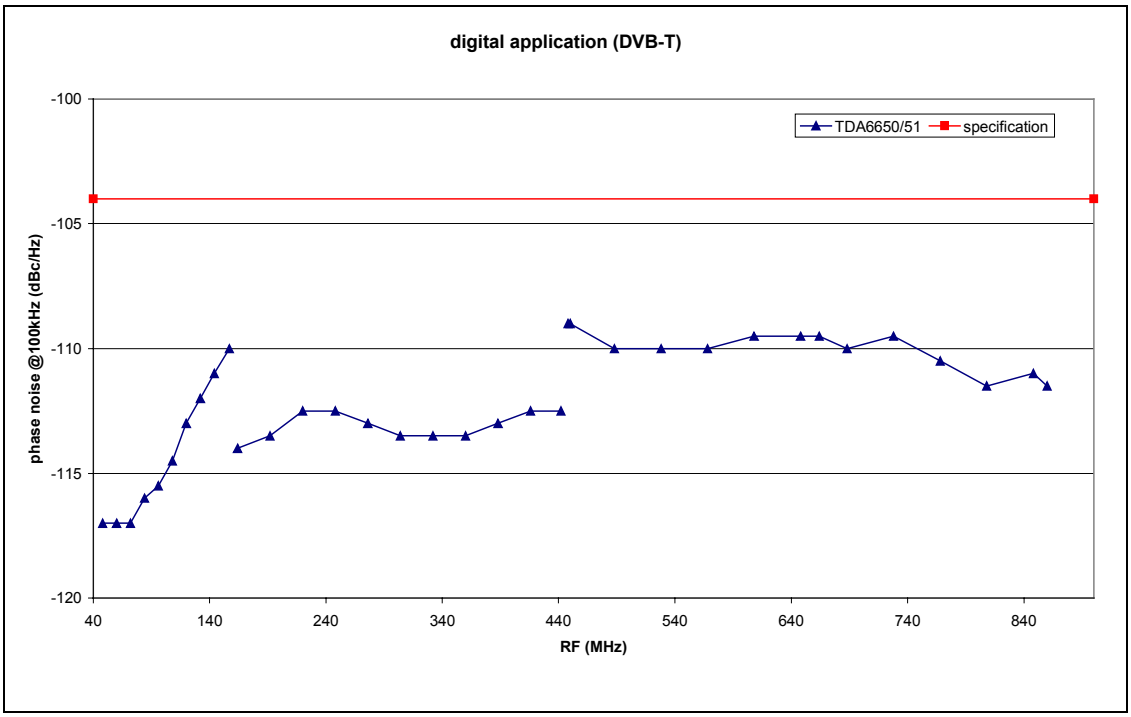


figure 11. 100kHz - phase noise measurement in the digital application (DVB-T).

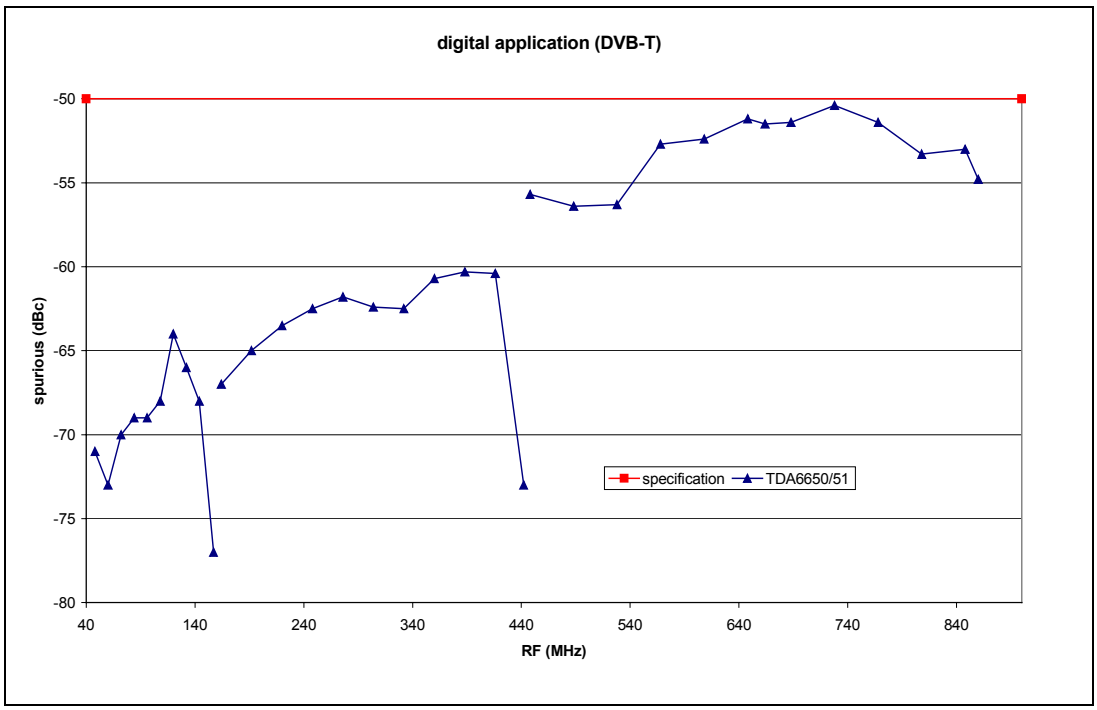


figure 12. 166.67kHz-spurious rejection measurement in the digital application (DVB-T).

Note: the charge-pump current table (Table 4) used for the phase noise and the spurious rejection measurements (DVB-T standard) is implemented in an embedded Read Only Memory (ROM). It is available thanks to the ALBC feature (see paragraph 3.4. ALBC in TDA6650/51TT).

3.2.2 hybrid applications (DVB-T & PAL standards)

An application, which targets the hybrid reception, should ensure a high step frequency spurious rejection in analogue mode and a low phase noise in digital mode. On the one hand, the frequency step spurious is rejected thanks to the filtering characteristics of the loop filter. On the other hand, the phase noise performance at 1kHz and 10kHz offsets is obtained if the PLL bandwidth is wide enough. A trade off between the two requirements has to be determined. Two hybrid applications will be described in this paper; the first one uses conventional loop filter architecture, in the second one the loop filter is switched depending on the reception mode.

3.2.2.1 Conventional filter (DVB-T & PAL standards)

● **Targeted performances**

The typical targeted performances are:

- Phase noise @1kHz = –80dBc/Hz.
- Phase noise @10kHz = –82dBc/Hz.
- Phase noise @100kHz = –104dBc/Hz.
- Frequency step spurious = –57dBc. (relative to the carrier)

● **Application**

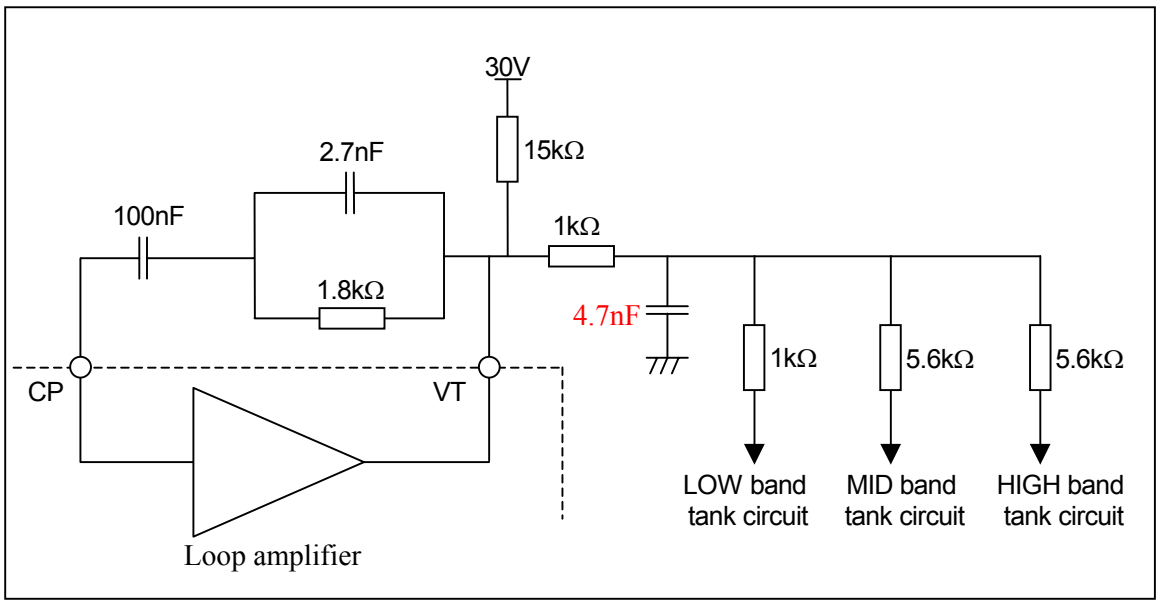


figure 13. Conventional loop filter for digital and analogue reception (DVB-T & PAL standards).

● **Digital reception with a conventional filter**

The conventional loop filter can be used in association with a charge-pump current table; this table also depends on the comparison frequency. All digital standards (166.67kHz, 142.86kHz and 125kHz) use the 4MHz comparison frequency; they are compatible with the following table.

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	80 to 128	44 to 92	190
	128 to 162	92 to 126	280
	162 to 171	126 to 135	410
	171 to 196	135 to 160	600
MID	196 to 255	160 to 219	130
	255 to 317	219 to 281	190
	317 to 372	281 to 336	280
	372 to 411	336 to 375	410
	411 to 482	375 to 446	600
HIGH	482 to 513	446 to 477	190
	513 to 676	477 to 640	280
	676 to 759	640 to 723	410
	759 to 902	723 to 866	600

Table 5. Charge-pump current programming for the 4MHz comparison frequency in the conventional hybrid application (DVB-T standard).

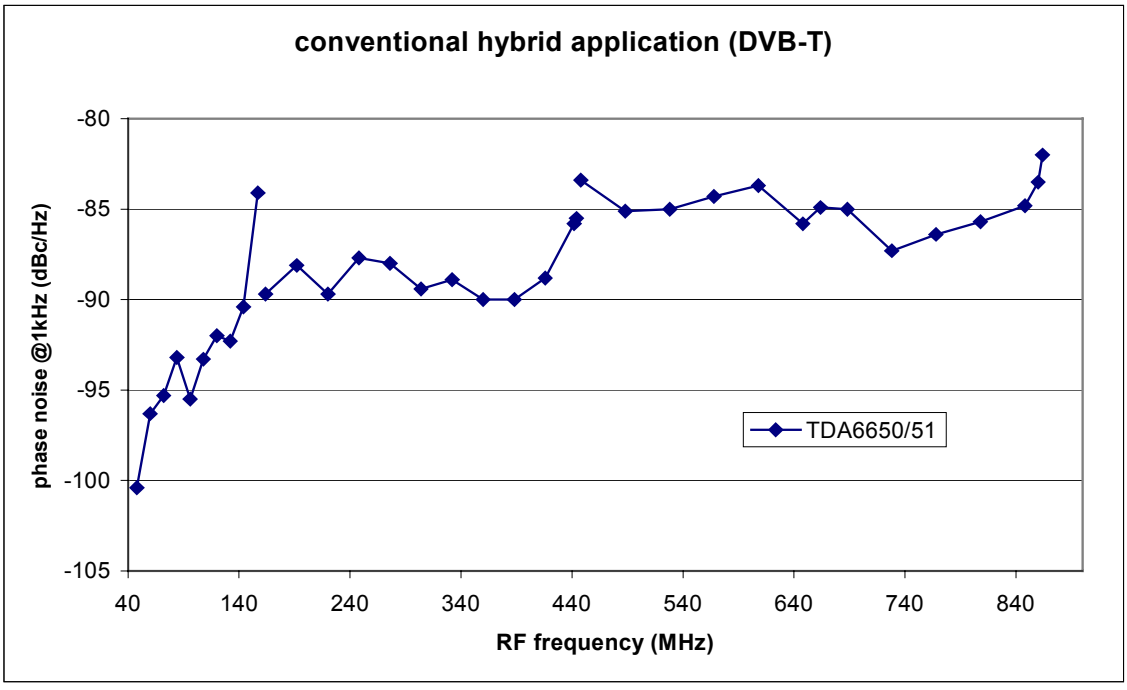


figure 14. 1kHz-phase noise measurement in the conventional hybrid application (DVB-T).

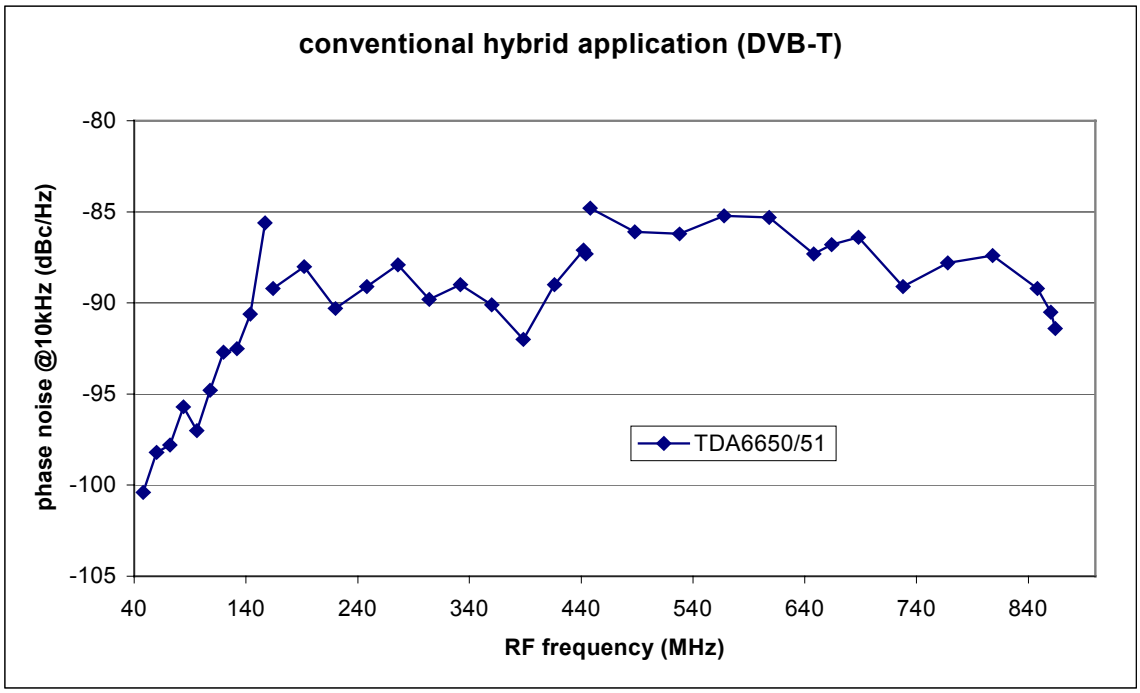


figure 15. 10kHz-phase noise measurement in the conventional hybrid application (DVB-T).

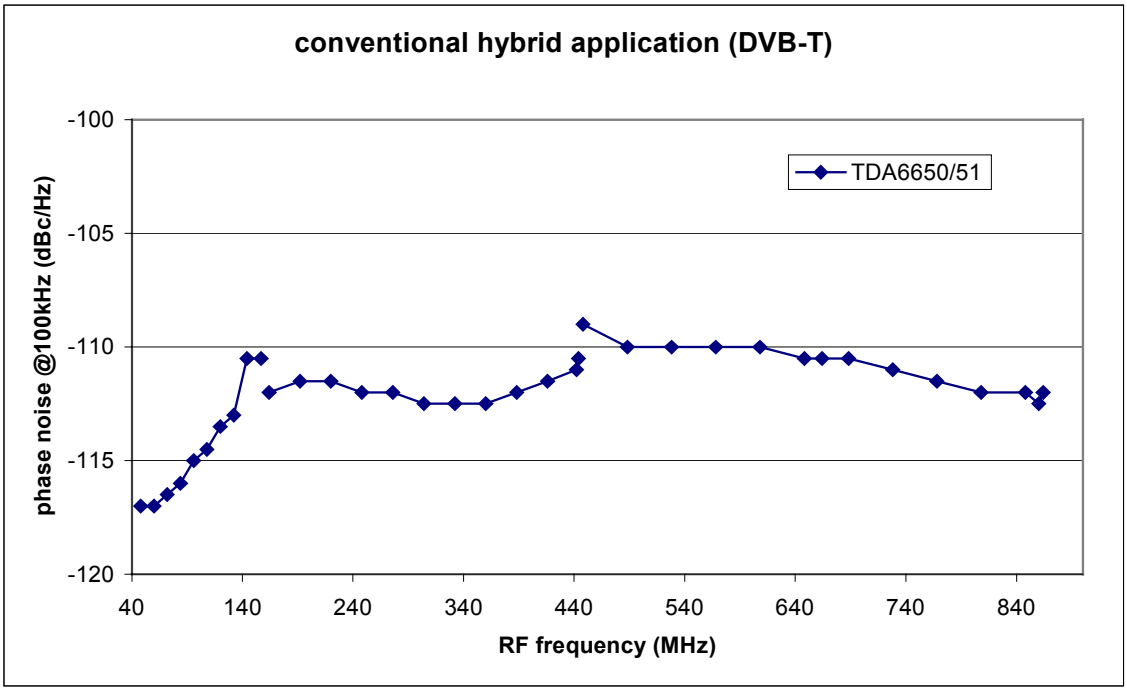


figure 16. 100kHz-phase noise measurement in the conventional hybrid application (DVBT).

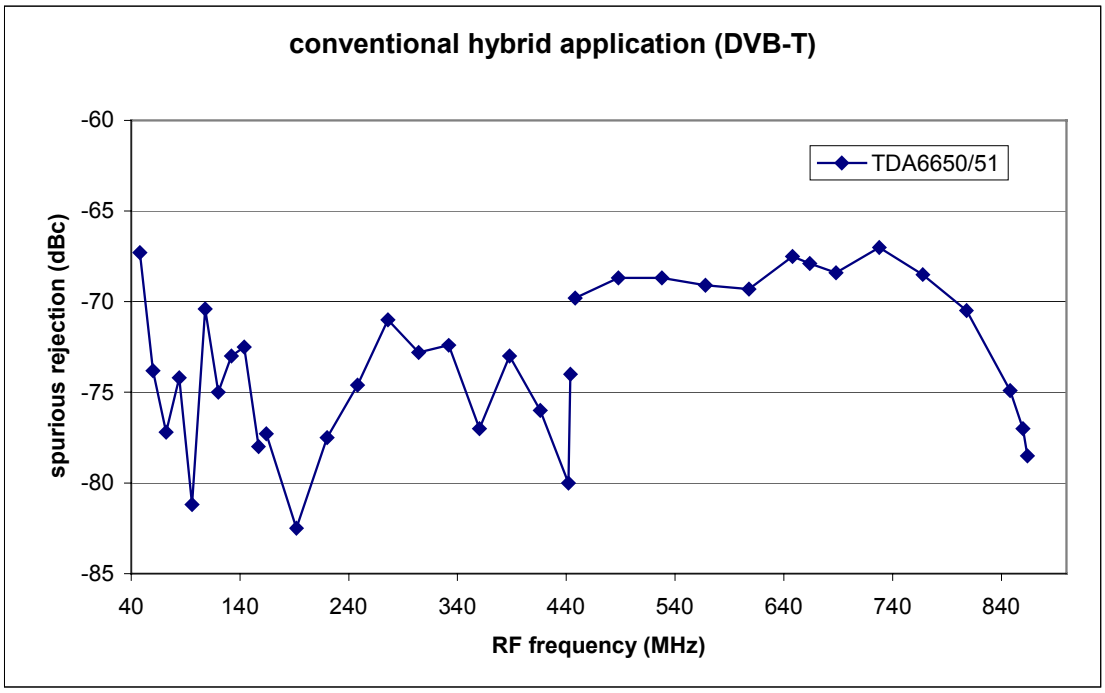


figure 17. 166.67kHz-spurious rejection measurement in the conventional hybrid application (DVB-T).

● **Analogue reception with a conventional filter**

Two comparison frequencies can be used for analogue reception; each one is associated to its table:

- 2MHz dedicated to analogue TV reception (frequency step 62.5kHz) → see Table 6.
- 1MHz dedicated to FM reception (frequency step 50kHz) → see Table 7.

band	osc (MHz)	RF (MHz)	charge pump current (uA)
	83,15 to 169	44,25 to 130,1	40
	169 to 179	130,1 to 140,1	60
	179 to 189	140,1 to 150,1	90
LOW	189 to 196,15	150,1 to 157,25	130
	196,15 to 406	157,25 to 367,1	40
	406 to 438	367,1 to 399,1	60
	438 to 461	399,1 to 422,1	90
MID	461 to 482,15	422,1 to 443,25	130
	482,15 to 750	443,25 to 711,1	40
	750 to 817	711,1 to 778,1	60
	817 to 862	778,1 to 823,1	90
	862 to 882	823,1 to 843,1	130
	882 to 895	843,1 to 856,1	190
HIGH	895 to 902,15	856,1 to 863,25	280

Table 6. Charge-pump current programming for the 2MHz comparison frequency in the conventional hybrid application.

band	osc (MHz)	RF (MHz)	charge pump current (uA)
	83,15 to 131	44,25 to 92,1	40
	131 to 162	92,1 to 123,1	60
	162 to 172	123,1 to 133,1	90
	172 to 182	133,1 to 143,25	130
	182 to 190	143,1 to 151,25	190
LOW	190 to 196,15	151,1 to 157,25	280
	196,15 to 320	157,25 to 281,1	40
	320 to 377	381,1 to 338,1	60
	377 to 417	338,1 to 378,1	90
	417 to 443	378,1 to 404,1	130
	443 to 464	404,1 to 425,1	190
MID	464 to 482,15	425,1 to 443,25	280
	482,15 to 518	443,25 to 479,1	40
	518 to 689	479,1 to 650,1	60
	689 to 772	650,1 to 733,1	90
	772 to 828	733,1 to 789,1	130
	828 to 865	789,1 to 826,1	190
	865 to 885	826,1 to 846,1	280
	865 to 896	846,1 to 857,1	410
HIGH	896 to 902,15	857,1 to 863,25	600

Table 7. Charge-pump current programming for the 1MHz comparison frequency in the conventional hybrid application.

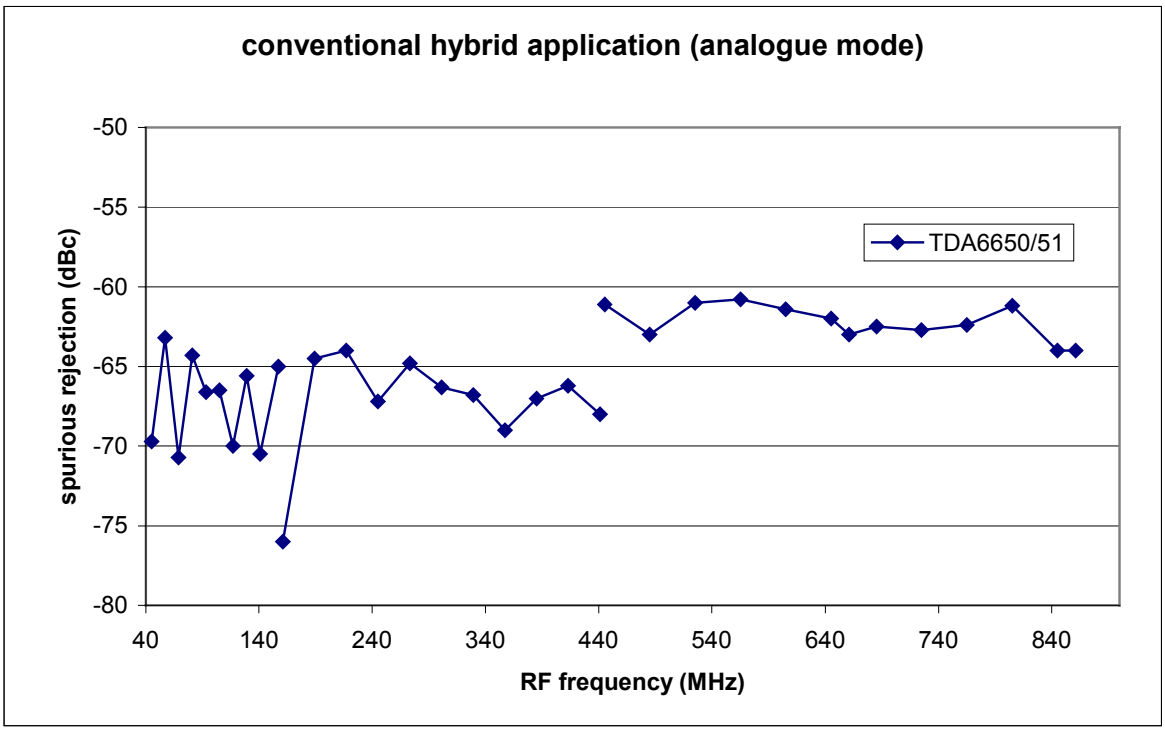


figure 18. 50kHz-spurious rejection measurement in the conventional hybrid application.

3.2.2.2 Switched concept (DVB-T & PAL standards)

The loop filter design constraints for analogue and digital reception are opposite, consequently, if the same loop filter is shared for both applications, a trade off has to be found. In practice, the previous conventional loop filter has been determined first to cope with the interference rejections (analogue mode); thus, the phase noise characteristics are lower than the theoretical optimum performance. In order to improve the phase noise, the following concept splits the filtering characteristics of the filter.

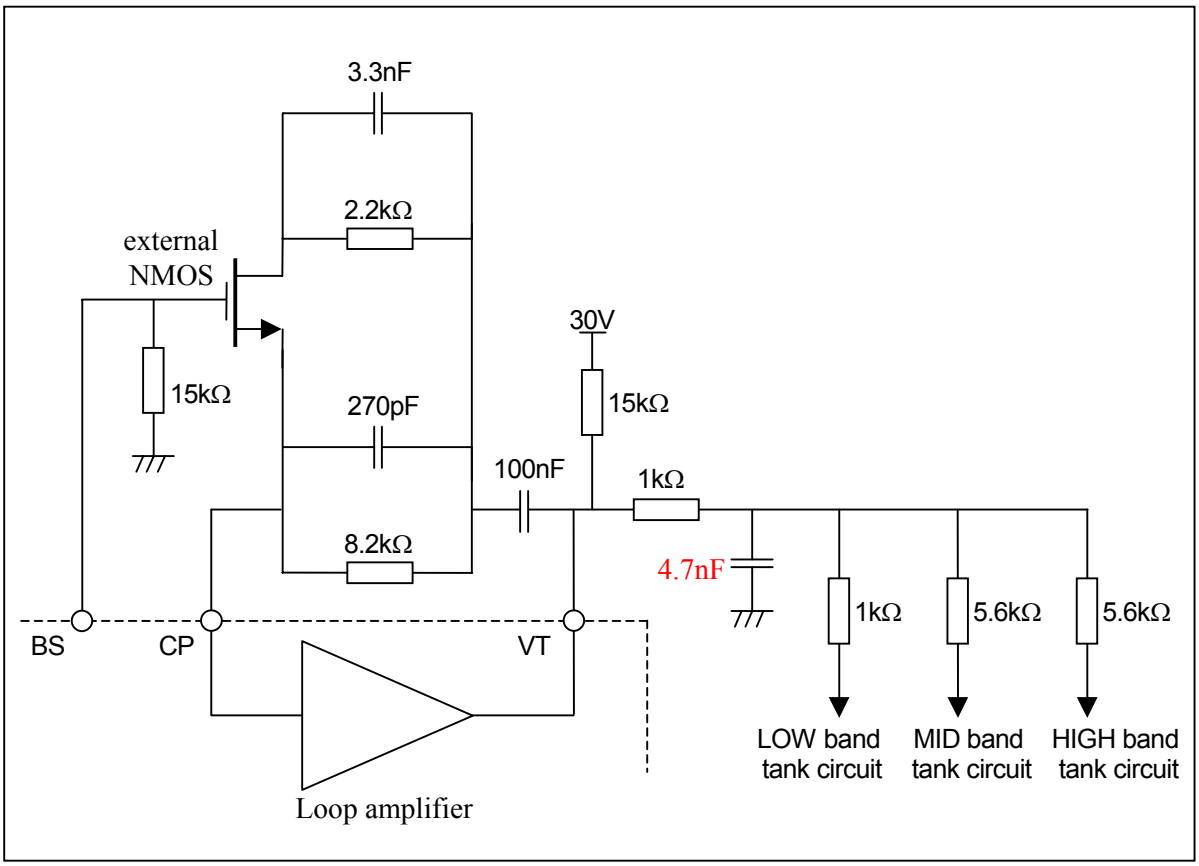


figure 19. Switched loop filter for digital and analogue reception (DVB-T & PAL standards).

Note: the external transistor used in the switched loop filter is a BSH111 NMOS.

- **Switched concept principle**
  - In case of digital reception, the output port BS is programmed OFF, consequently, the external NMOS transistor is switched OFF: the gate voltage is 0V. Therefore the transistor presents a high impedance to the charge–pump output, the 2.2kΩ resistor and the 3.3nF capacitance are disconnected. The loop filter can be simplified as follows:

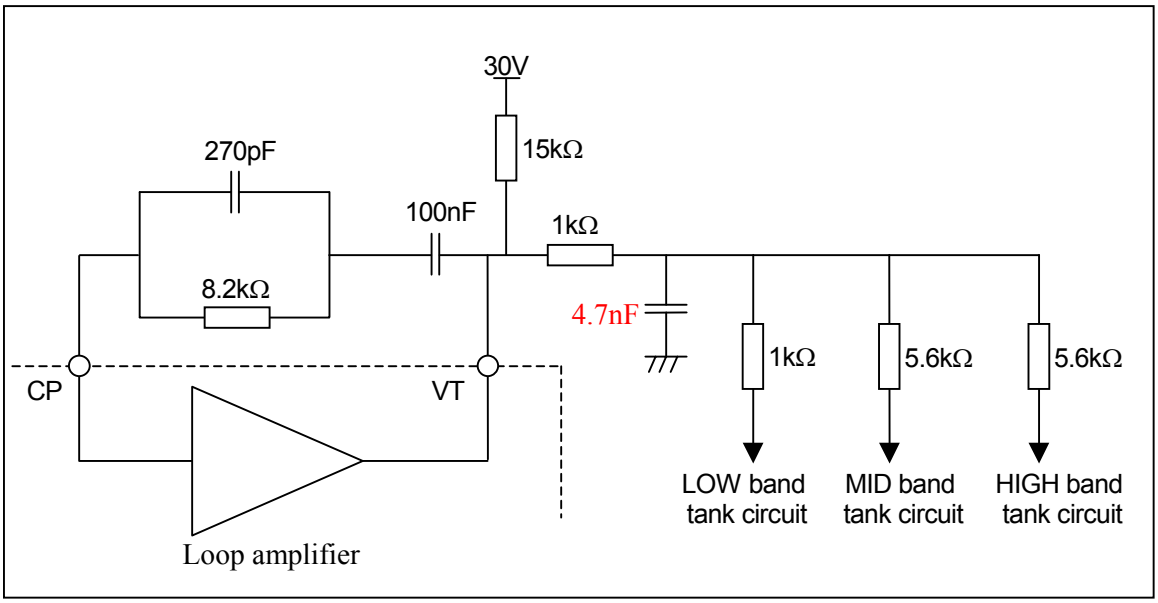


figure 20. Simplified view of the switched filter in case of digital reception.

- On the opposite, when receiving an analogue channel, BS is switched ON, thus the gate voltage is higher than 4.6V (5V – $V_{ds,sat}$). The NMOS is switched ON, and presents a low impedance $R_{ds,on}$, the 2.2kΩ resistor and the 3.3nF capacitance are connected in parallel with the 8.2kΩ resistor and the 270pF capacitance. The schematic can be simplified as follows:

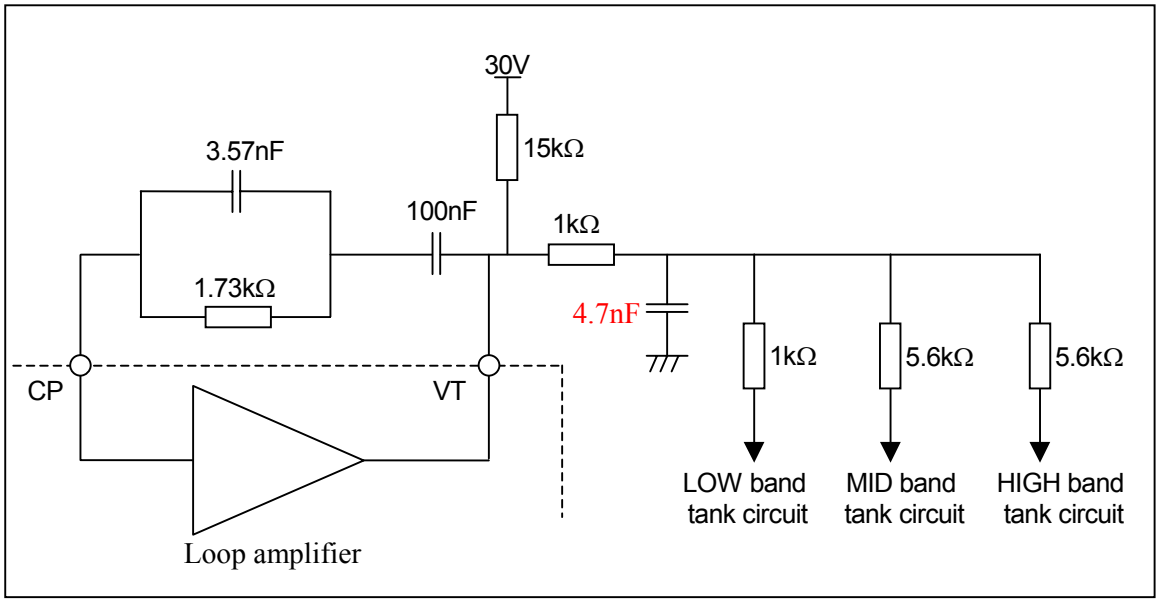


figure 21. Simplified view of the switched filter in case of analogue reception.

- **Digital reception with the switched filter.**

band	osc (MHz)	RF (MHz)	charge pump current (uA)
	80 to 157	44 to 121	90
	157 to 168	121 to 132	130
	168 to 178	132 to 142	190
	178 to 188	142 to 152	280
	188 to 194	152 to 158	410
LOW	194 to 196	158 to 160	600
	196 to 303	160 to 267	60
	303 to 356	267 to 320	90
	356 to 400	320 to 364	130
	400 to 432	364 to 396	190
	432 to 456	396 to 420	280
MID	456 to 482	420 to 446	410
	482 to 637	446 to 601	90
	637 to 736	601 to 700	130
	736 to 804	700 to 768	190
	804 to 853	768 to 817	280
	853 to 878	817 to 842	410
HIGH	878 to 902	842 to 866	600

Table 8. Charge-pump current programming for 4MHz comparison frequency in the switched application (DVB-T standard).

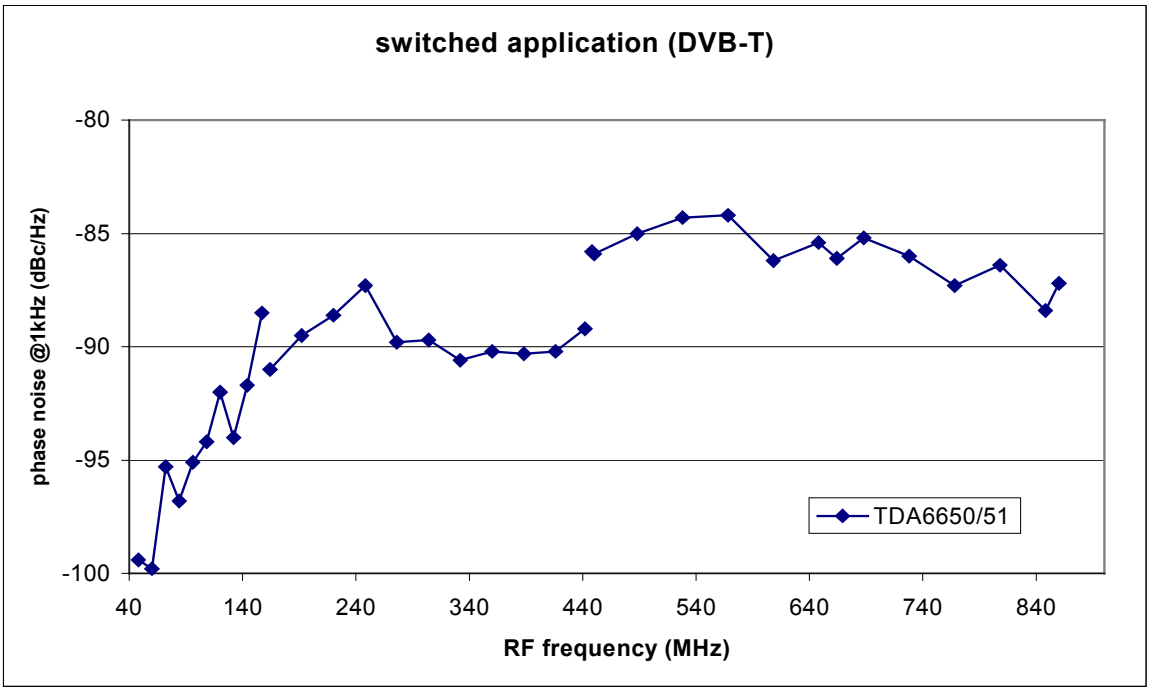


figure 22. 1kHz-phase noise measurement in the switched application (DVB-T).

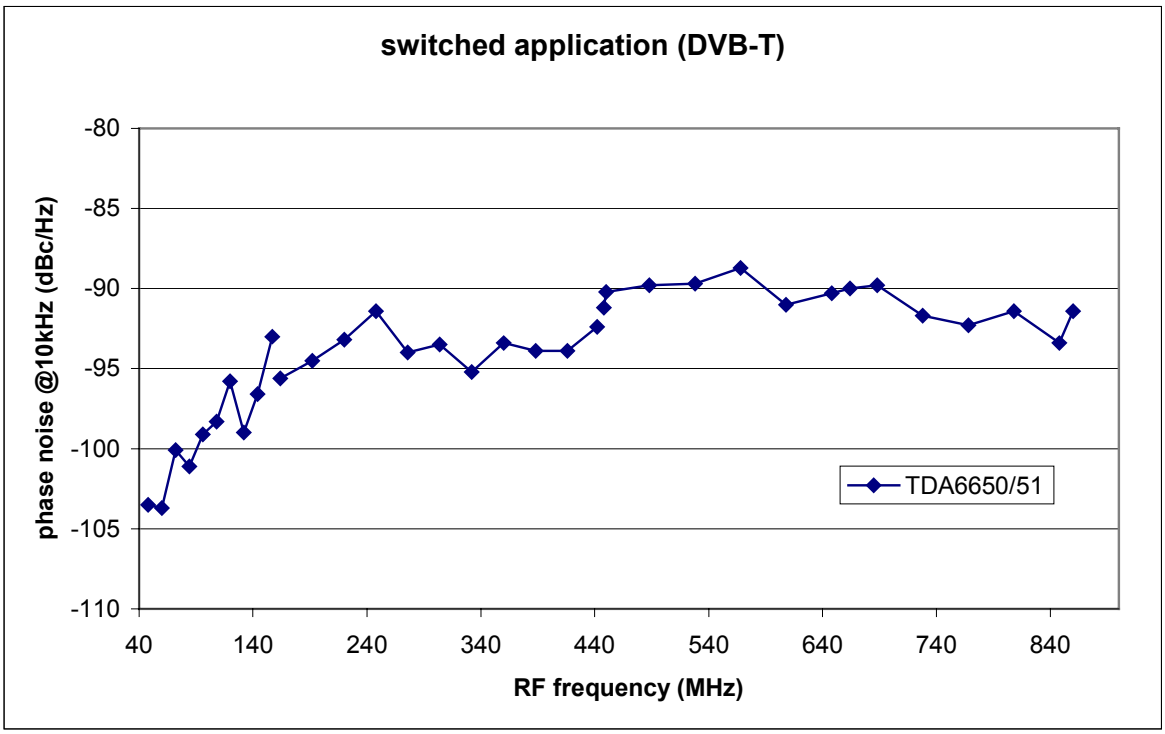


figure 23. 10kHz-phase noise measurement in the switched application (DVB-T).

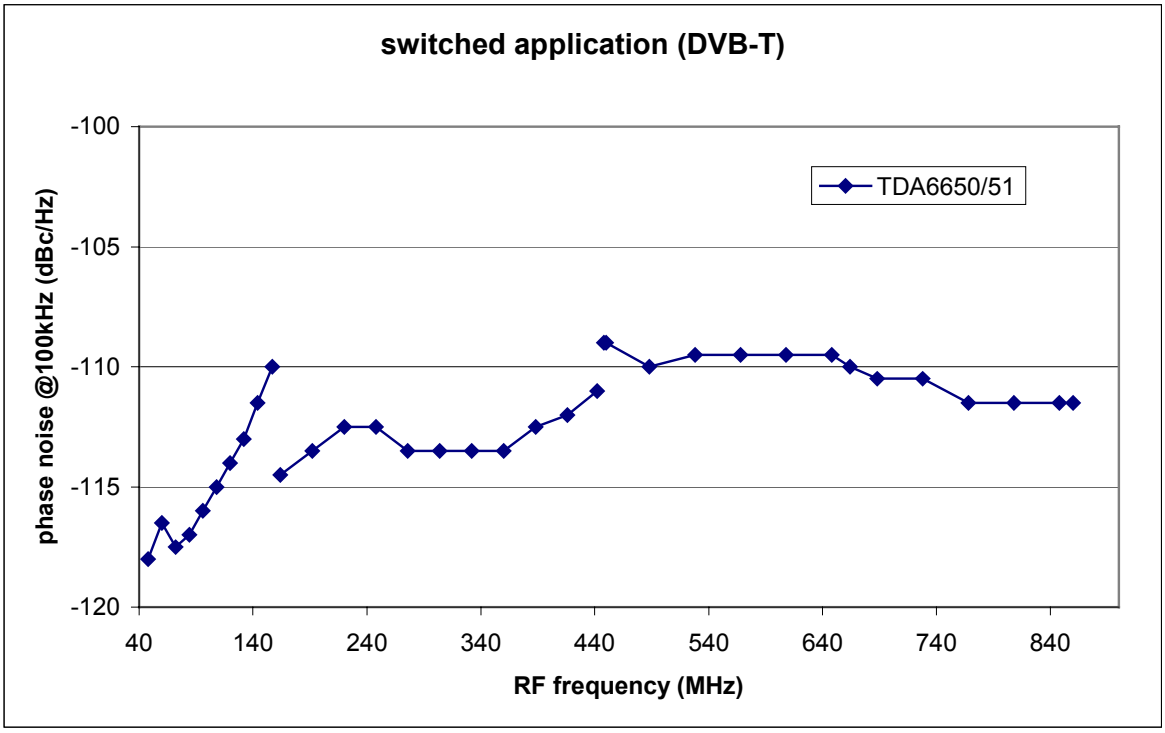


figure 24. 100kHz-phase noise measurement in the switched application (DVB-T).

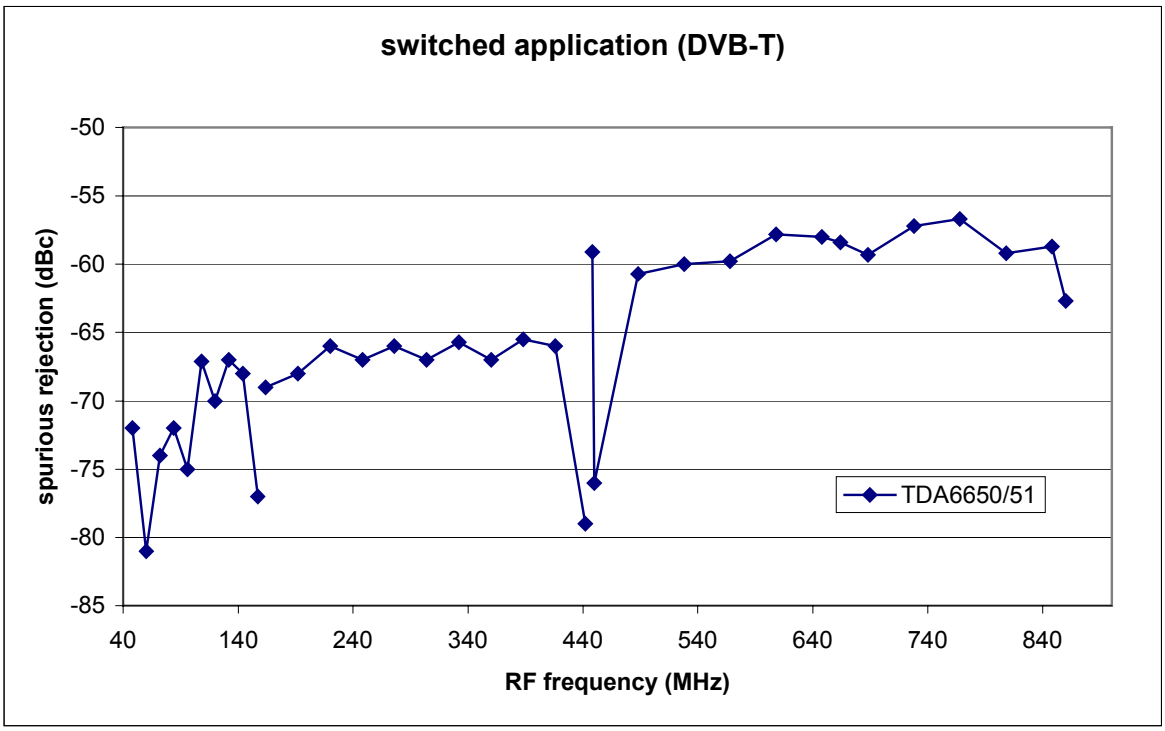


figure 25. 166.67kHz-spurious rejection measurement in the switched application (DVB-T).

- **Analogue reception with switched application**

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	83,15 to 169	44,25 to 130,1	40
	169 to 179	130,1 to 140,1	60
	179 to 189	140,1 to 150,1	90
	189 to 196,15	150,1 to 157,25	130
MID	196,15 to 406	157,25 to 367,1	40
	406 to 438	367,1 to 399,1	60
	438 to 461	399,1 to 422,1	90
	461 to 482,15	422,1 to 443,25	130
HIGH	482,15 to 750	443,25 to 711,1	40
	750 to 817	711,1 to 778,1	60
	817 to 862	778,1 to 823,1	90
	862 to 882	823,1 to 843,1	130
	882 to 895	843,1 to 856,1	190
	895 to 902,15	856,1 to 863,25	280

Table 9. Charge-pump current programming for the 2MHz comparison frequency in the switched application.

NB: The Table 9 is identical to the Table 6 (charge-pump current programming for the 2MHz comparison frequency in the conventional hybrid application).

band	osc (MHz)	RF (MHz)	charge pump current (uA)
	83,15 to 131	44,25 to 92,1	40
	131 to 162	92,1 to 123,1	60
	162 to 172	123,1 to 133,1	90
	172 to 182	133,1 to 143,25	130
	182 to 190	143,1 to 151,25	190
LOW	190 to 196,15	151,1 to 157,25	280
	196,15 to 320	157,25 to 281,1	40
	320 to 377	381,1 to 338,1	60
	377 to 417	338,1 to 378,1	90
	417 to 443	378,1 to 404,1	130
	443 to 464	404,1 to 425,1	190
MID	464 to 482,15	425,1 to 443,25	280
	482,15 to 518	443,25 to 479,1	40
	518 to 689	479,1 to 650,1	60
	689 to 772	650,1 to 733,1	90
	772 to 828	733,1 to 789,1	130
	828 to 865	789,1 to 826,1	190
	865 to 885	826,1 to 846,1	280
	865 to 896	846,1 to 857,1	410
HIGH	896 to 902,15	857,1 to 863,25	600

Table 10. Charge-pump current programming for the 1MHz comparison frequency in the switched application.

NB: The Table 10 is identical to the Table 7 (charge-pump current programming for the 1MHz comparison frequency in the conventional hybrid application).

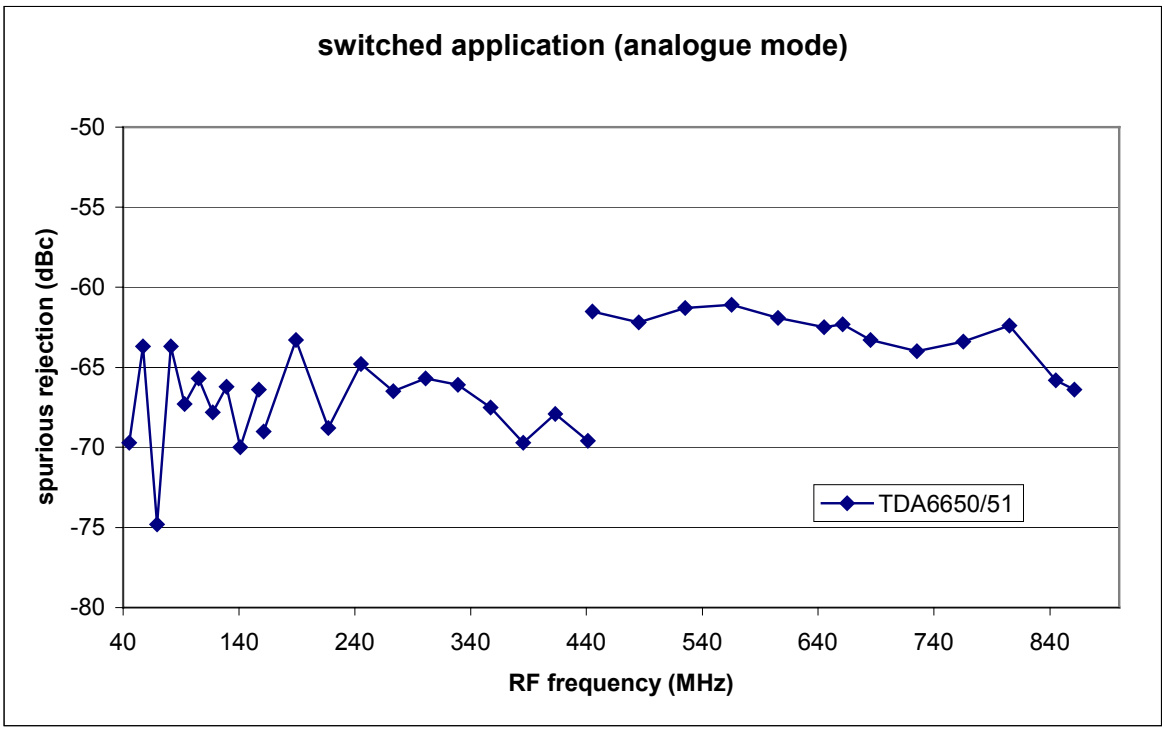


figure 26. 50kHz-spurious rejection measurement in the switched application (analogue).

3.3 Loop filter application for NTSC Japan & ISDB-T standards

● **Validity domain**

The present chapter is dedicated to the Japanese standards (NTSC Japan & ISDB-T standards). All measurements and simulations were performed with local oscillators tuned with respect to the figure 27. The frequency coverage is defined in the Table 11.

If the oscillators are tuned with different ranges, the measurement results may change (some other optimizations can be necessary).

The IF intermediate frequencies programmed for the measurements are:

- 57MHz ISDB-T application.
- 58.75MHz NTSC Japan application.

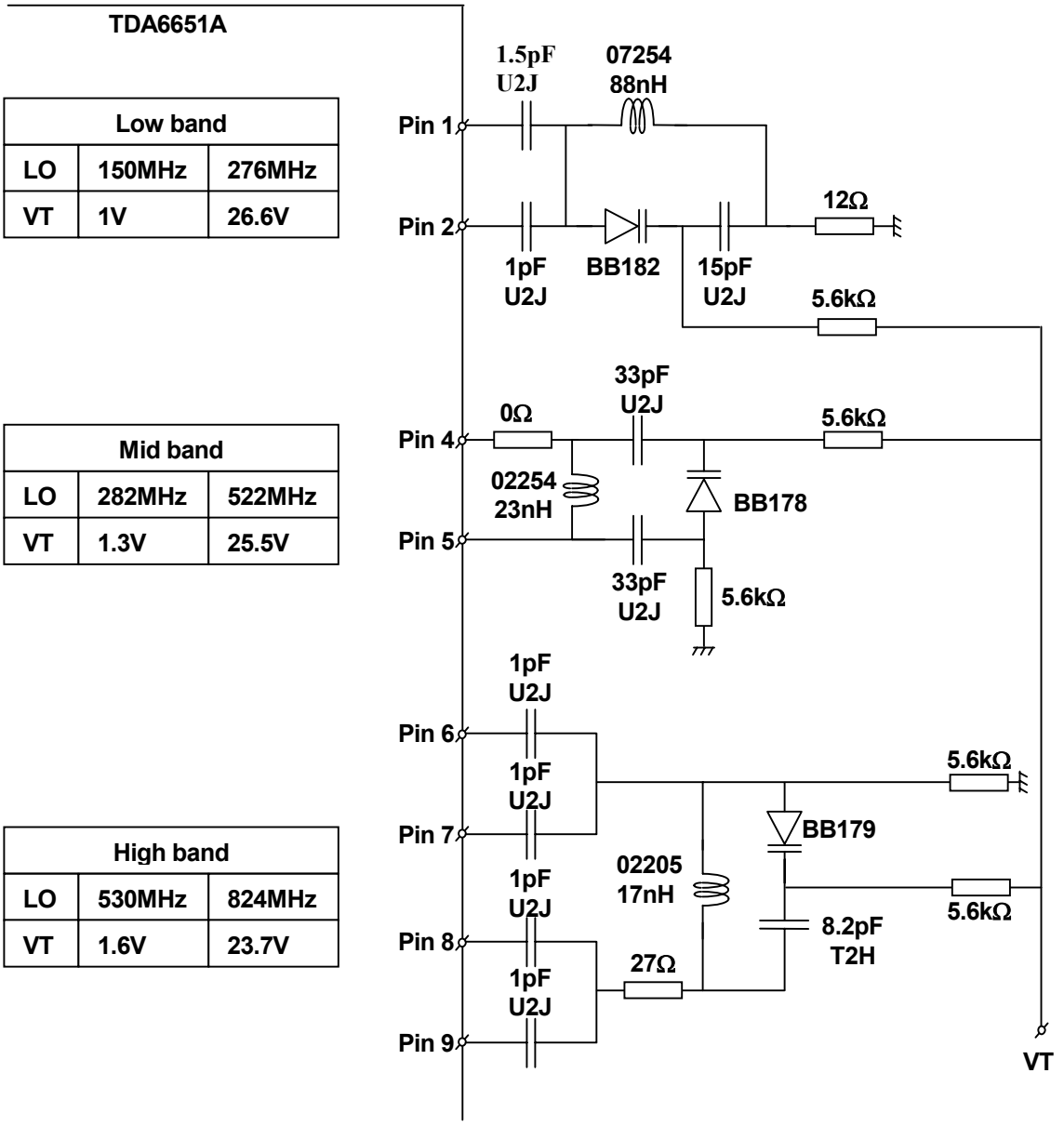


figure 27. Oscillators tank circuits used for the measurements (Japanese market).

LOW BAND			MID BAND			HIGH BAND		
channel	RF frequency (MHz)	LO frequency (MHz)	channel	RF frequency (MHz)	LO frequency (MHz)	channel	RF frequency (MHz)	LO frequency (MHz)
1	93,14286	150,1429	C23	225,1429	282,1429	13	473,1429	530,1429
2	99,14286	156,1429	C24	231,1429	288,1429	14	479,1429	536,1429
3	105,1429	162,1429	C25	237,1429	294,1429	15	485,1429	542,1429
C13	111,1429	168,1429	C26	243,1429	300,1429	16	491,1429	548,1429
C14	117,1429	174,1429	C27	249,1429	306,1429	17	497,1429	554,1429
C15	123,1429	180,1429	C28	255,1429	312,1429	18	503,1429	560,1429
C16	129,1429	186,1429	C29	261,1429	318,1429	19	509,1429	566,1429
C17	135,1429	192,1429	C30	267,1429	324,1429	20	515,1429	572,1429
C18	141,1429	198,1429	C31	273,1429	330,1429	21	521,1429	578,1429
C19	147,1429	204,1429	C32	279,1429	336,1429	22	527,1429	584,1429
C20	153,1429	210,1429	C33	285,1429	342,1429	23	533,1429	590,1429
C21	159,1429	216,1429	C34	291,1429	348,1429	24	539,1429	596,1429
C22	165,1429	222,1429	C35	297,1429	354,1429	25	545,1429	602,1429
4	171,1429	228,1429	C36	303,1429	360,1429	26	551,1429	608,1429
5	177,1429	234,1429	C37	309,1429	366,1429	27	557,1429	614,1429
6	183,1429	240,1429	C38	315,1429	372,1429	28	563,1429	620,1429
7	189,1429	246,1429	C39	321,1429	378,1429	29	569,1429	626,1429
8	195,1429	252,1429	C40	327,1429	384,1429	30	575,1429	632,1429
9	201,1429	258,1429	C41	333,1429	390,1429	31	581,1429	638,1429
10	207,1429	264,1429	C42	339,1429	396,1429	32	587,1429	644,1429
11	213,1429	270,1429	C43	345,1429	402,1429	33	593,1429	650,1429
12	219,1429	276,1429	C44	351,1429	408,1429	34	599,1429	656,1429
			C45	357,1429	414,1429	35	605,1429	662,1429
			C46	363,1429	420,1429	36	611,1429	668,1429
			C47	369,1429	426,1429	37	617,1429	674,1429
			C48	375,1429	432,1429	38	623,1429	680,1429
			C49	381,1429	438,1429	39	629,1429	686,1429
			C50	387,1429	444,1429	40	635,1429	692,1429
			C51	393,1429	450,1429	41	641,1429	698,1429
			C52	399,1429	456,1429	42	647,1429	704,1429
			C53	405,1429	462,1429	43	653,1429	710,1429
			C54	411,1429	468,1429	44	659,1429	716,1429
			C55	417,1429	474,1429	45	665,1429	722,1429
			C56	423,1429	480,1429	46	671,1429	728,1429
			C57	429,1429	486,1429	47	677,1429	734,1429
			C58	435,1429	492,1429	48	683,1429	740,1429
			C59	441,1429	498,1429	49	689,1429	746,1429
			C60	447,1429	504,1429	50	695,1429	752,1429
			C61	453,1429	510,1429	51	701,1429	758,1429
			C62	459,1429	516,1429	52	707,1429	764,1429
			C63	465,1429	522,1429	53	713,1429	770,1429
						54	719,1429	776,1429
						55	725,1429	782,1429
						56	731,1429	788,1429
						57	737,1429	794,1429
						58	743,1429	800,1429
						59	749,1429	806,1429
						60	755,1429	812,1429
						61	761,1429	818,1429
						62	767,1429	824,1429

Table 11. Channel frequency coverage (Japanese standard).

The local oscillator characteristic (slope) is given in the figure 28.

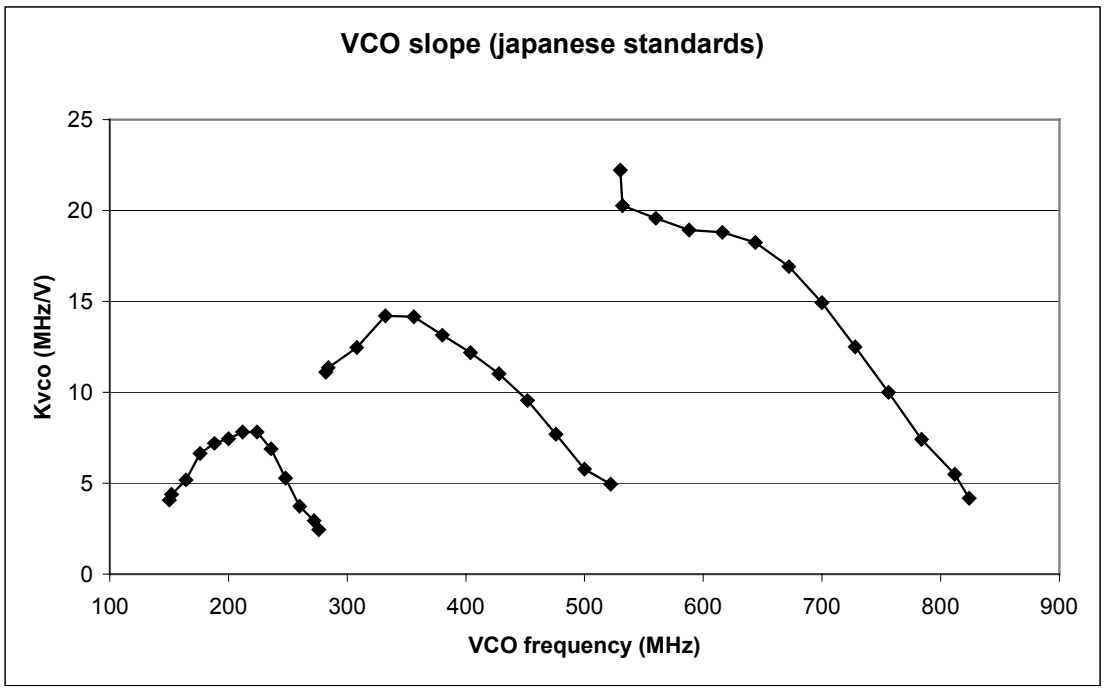


figure 28. VCO characteristics (Japanese standard).

3.3.1 Pure digital application (ISDB-T standard)

● **Specification points**

Two main parameters are used to design the MOPLL application:

- The phase noise performance.
- The spurious rejection.

The minimum performances are:

- Phase noise @1kHz < –80dBc/Hz.
- Phase noise @10kHz < –85dBc/Hz.
- Frequency step spurious (142.86kHz)< –50dBc. (relative to the carrier)

● **Digital application - software programming**

A loop filter application in association with a charge-pump table determines the PLL loop characteristics. First of all, the loop filter should guaranty the system stability (phase margin), then, it has to fulfil the appropriate PLL bandwidth to reach the required spurious rejection and also to allow a low synthesizer noise floor:

1. The loop stability is obtained provided the phase margin of the PLL second order loop is high enough. All the filters presented in this chapter ensure a phase margin of 38° (worst case).
2. The phase noise performances are reached by designing a loop filter that adjusts the PLL bandwidth.

Note: for every application a single optimized charge-pump table can be simulated.

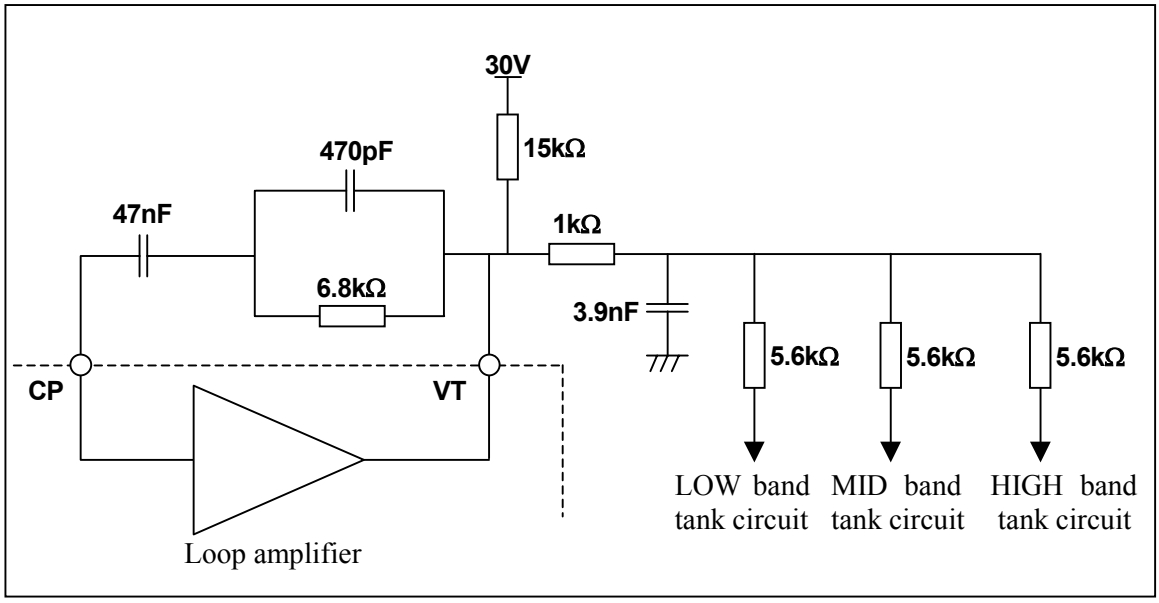


figure 29. Loop filter for pure digital application (ISDB-T standard).

The TDA6650/51 is able to synthesize a Local Oscillator frequency with 5 different steps. In the fractional architecture those 5 different steps corresponds to 3 comparison frequencies. The loop filter design is only affected by the comparison frequency; therefore a charge-pump current table is linked to the comparison frequency in use. The table below is dedicated to the digital reception therefore to the 4MHz comparison frequency (frequency step 125kHz, 142.86kHz and 166.67kHz).

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 170	93 to 113	190
	170 to 218	113 to 161	130
	218 to 242	161 to 185	190
	242 to 254	185 to 197	280
	254 to 274	197 to 217	410
	274 to 276,143	217 to 219,143	600
MID	282 to 368	225 to 311	130
	368 to 440	311 to 383	190
	440 to 488	383 to 431	280
	488 to 511	431 to 454	410
	511 to 522,143	454 to 465,143	600
HIGH	530 to 546	473 to 489	130
	546 to 686	489 to 629	190
	686 to 742	629 to 685	280
	742 to 770	685 to 713	410
	770 to 824,143	713 to 767,143	600

Table 12. Charge-pump current programming for the 4MHz comparison frequency in the digital application (ISDB-T standard).

All the measurements described in this paper where performed on the TDA6651 demonstration board (PCB 827-3), the oscillators tank circuits are defined figure 27.

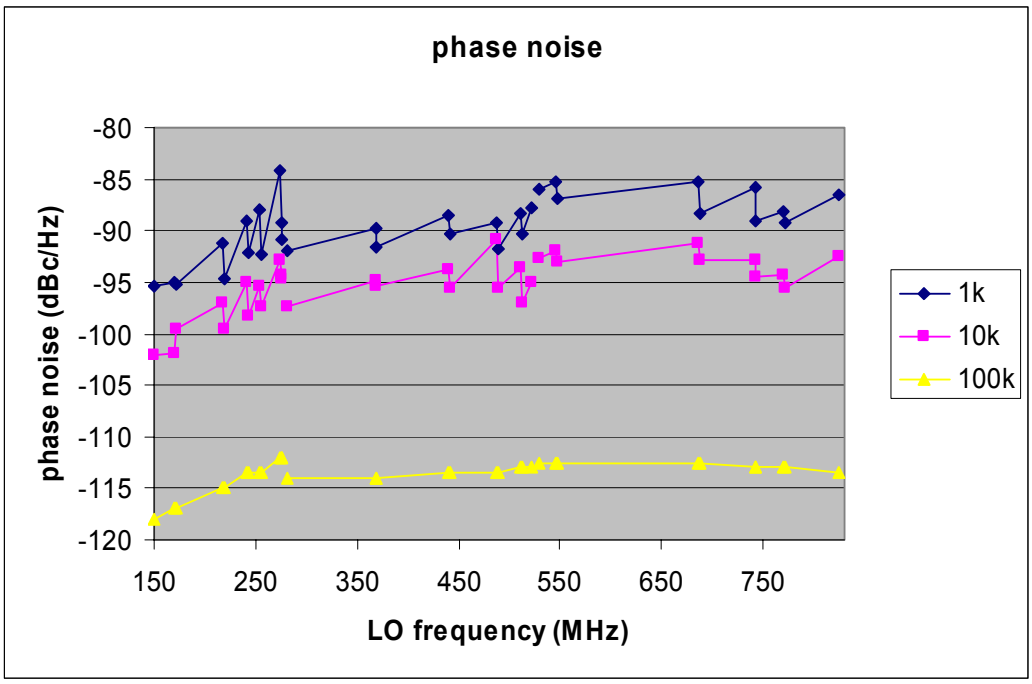


figure 30. Phase noise measurement in the digital application (ISDB-T).

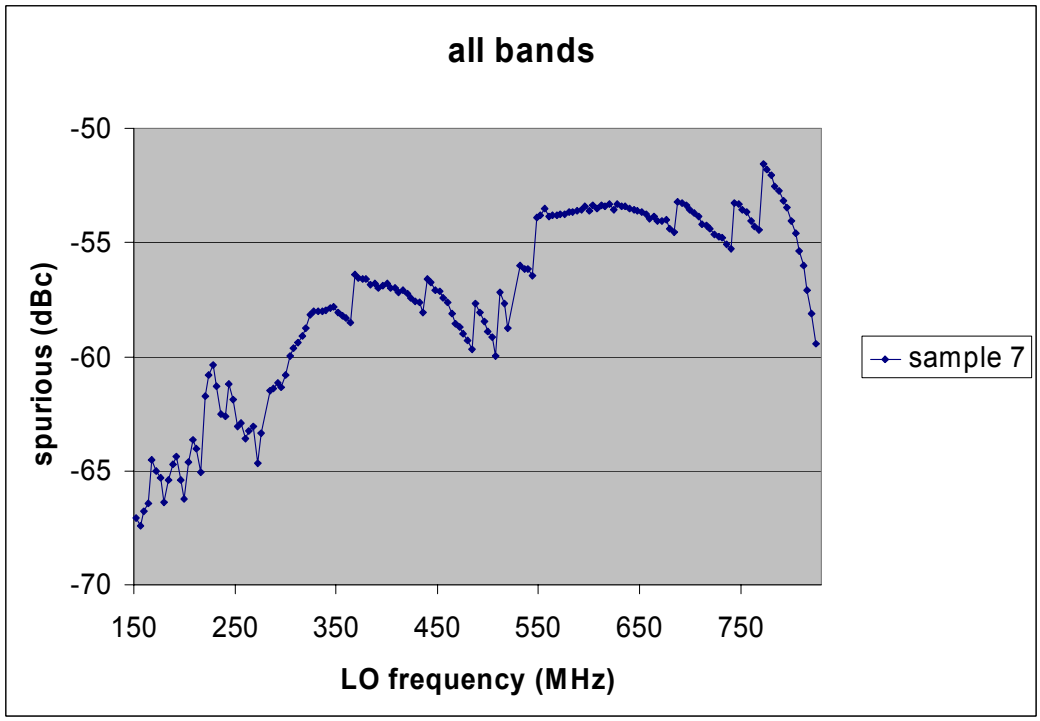


figure 31. 142.86kHz-spurious rejection measurement in the digital application (ISDB-T).

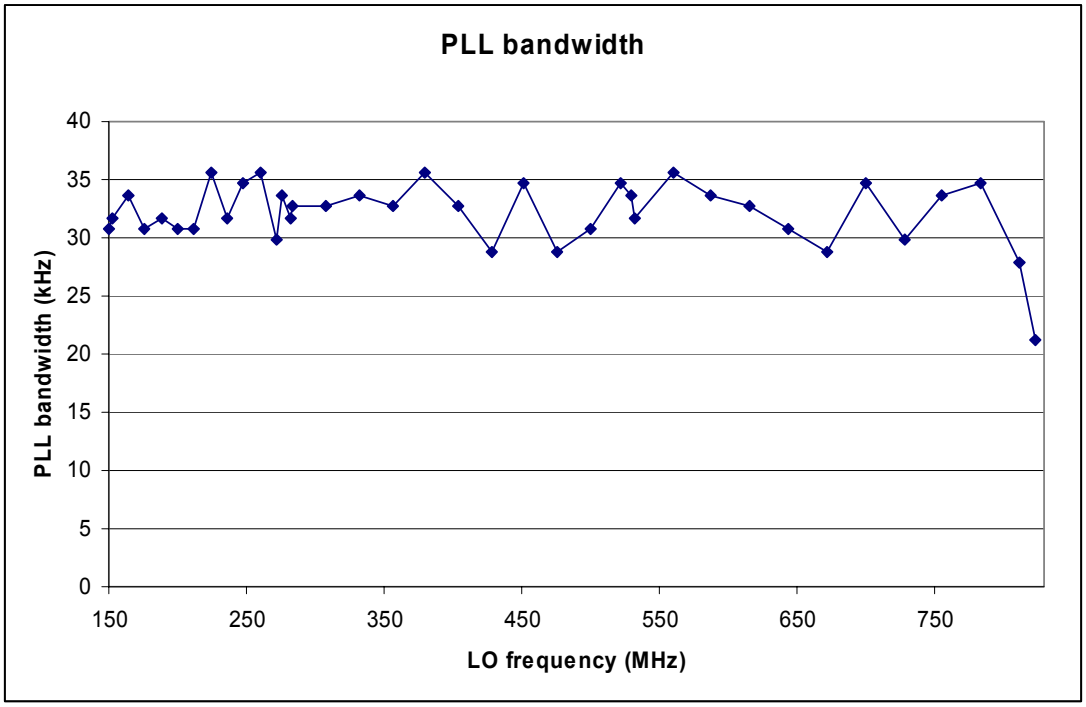


figure 32. PLL bandwidth in the digital application (ISDB-T)

3.3.2 hybrid applications (ISDB-T & NTSC Japan standards)

An application, which targets the hybrid reception, should ensure a high spurious rejection in analogue mode and a low phase noise in digital mode. On the one hand, the frequency step spurious is rejected thanks to the filtering characteristics of the loop filter. On the other hand, the phase noise performance at 1kHz and 10kHz offsets is obtained if the PLL bandwidth is wide enough. A trade off between the two requirements has to be determined. Two hybrid applications will be described in this paper; the first one uses conventional loop filter architecture, in the second one the loop filter is switched depending on the reception mode.

3.3.2.1 Conventional filter

- **Targeted performances**

The minimum performances are:

- Phase noise @1kHz < –75dBc/Hz.
- Phase noise @10kHz < –82dBc/Hz.
- Frequency step spurious < –57dBc. (relative to the carrier)

● Application

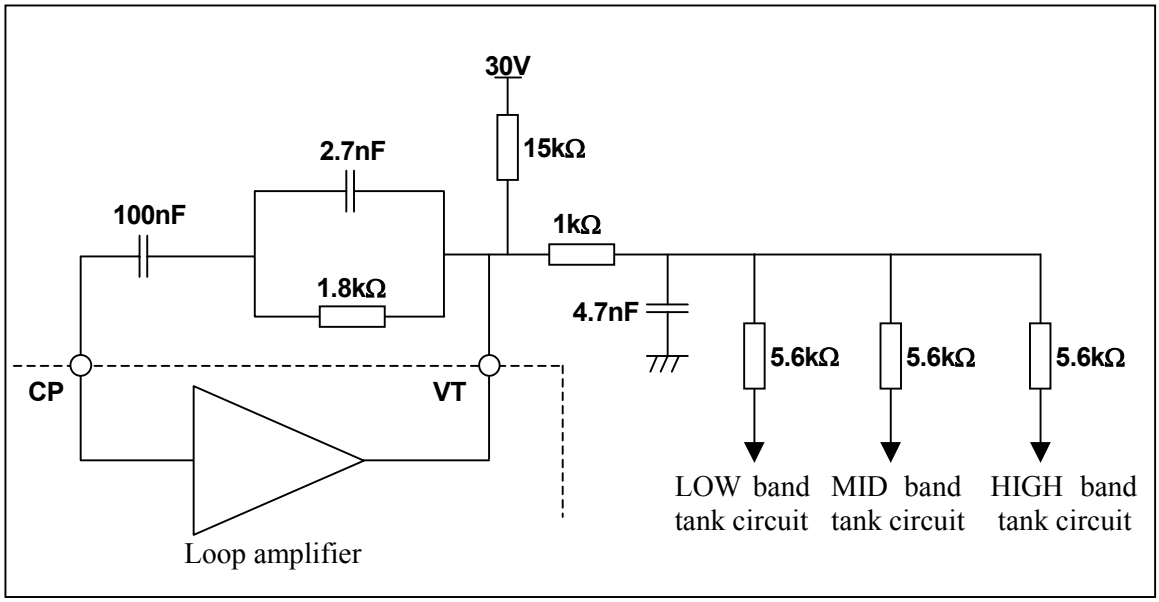


figure 33. Conventional loop filter for digital and analogue reception (ISDB-T & NTSC Japan standards).

● Digital reception with a conventional filter

The conventional loop filter can be used in association with a charge-pump current table; this table also depends on the comparison frequency. All digital standards (166.67kHz, 142.86kHz and 125kHz) use the 4MHz comparison frequency; they are compatible with the following table.

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 170 170 to 218 218 to 242 242 to 276,143	93 to 113 113 to 161 161 to 185 185 to 219,143	410 280 410 600
MID	282 to 368 368 to 440 440 to 522,143	225 to 311 311 to 383 383 to 465,143	280 410 600
HIGH	530 to 546 546 to 686 686 to 824,143	473 to 489 489 to 629 629 to 767,143	280 410 600

Table 13. Charge-pump current programming for the 4MHz comparison frequency in the conventional hybrid application (ISDB-T standard).

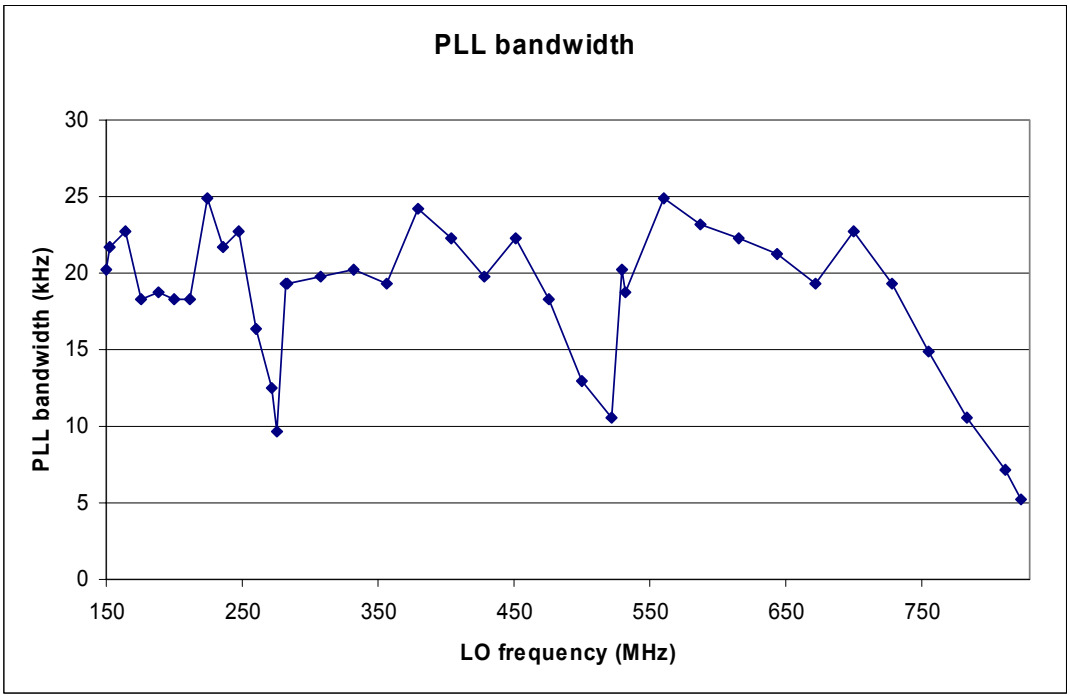


figure 34. PLL bandwidth in the conventional application (fstep=142.86kHz).

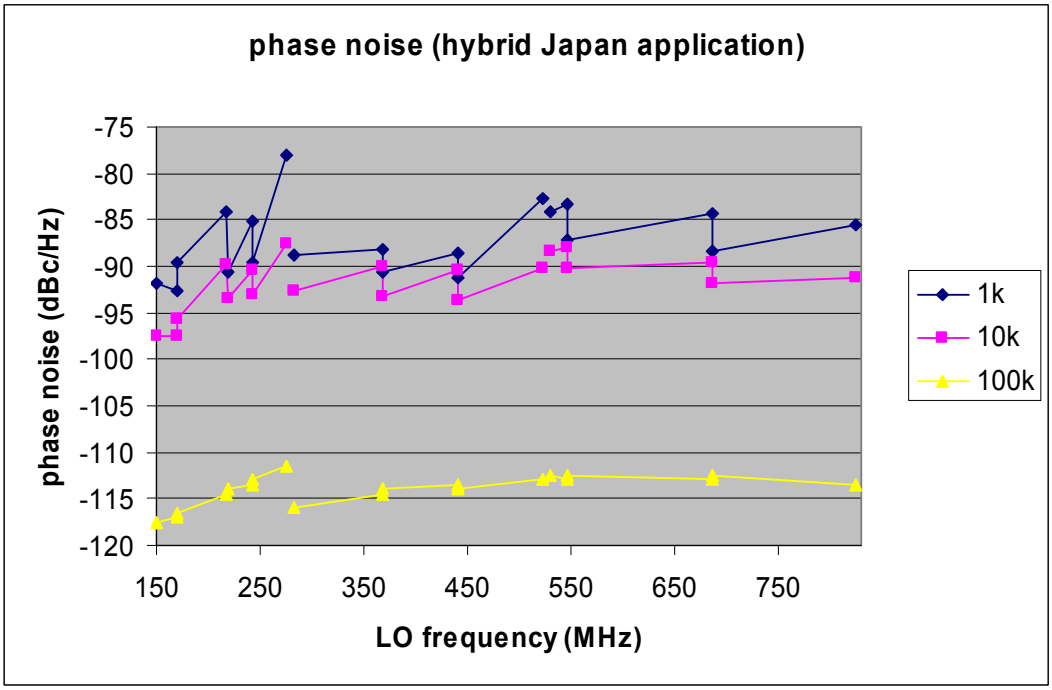


figure 35. Phase noise measurement in the conventional hybrid application (ISDB-T).

- **Analogue reception with a conventional filter**

Two comparison frequencies can be used for analogue reception; each one is associated to its table:

- 2MHz dedicated to analogue TV reception (frequency step 62.5kHz) → see Table 14
- 1MHz dedicated to FM reception (frequency step 50kHz) → see Table 15
-

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 242	93 to 185	40
	242 to 254	185 to 197	60
	254 to 266	197 to 209	90
	266 to 276,143	209 to 219,143	130
MID	282 to 416	225 to 359	40
	416 to 464	359 to 407	60
	464 to 488	407 to 431	90
	488 to 522,143	431 to 465,143	130
HIGH	530 to 658	473 to 601	40
	658 to 714	601 to 657	60
	714 to 770	657 to 713	90
	770 to 798	713 to 741	130
	798 to 818	741 to 761	190
	818 to 824,143	761 to 767,143	280

Table 14. Charge-pump current programming for the 2MHz comparison frequency in the conventional hybrid application.

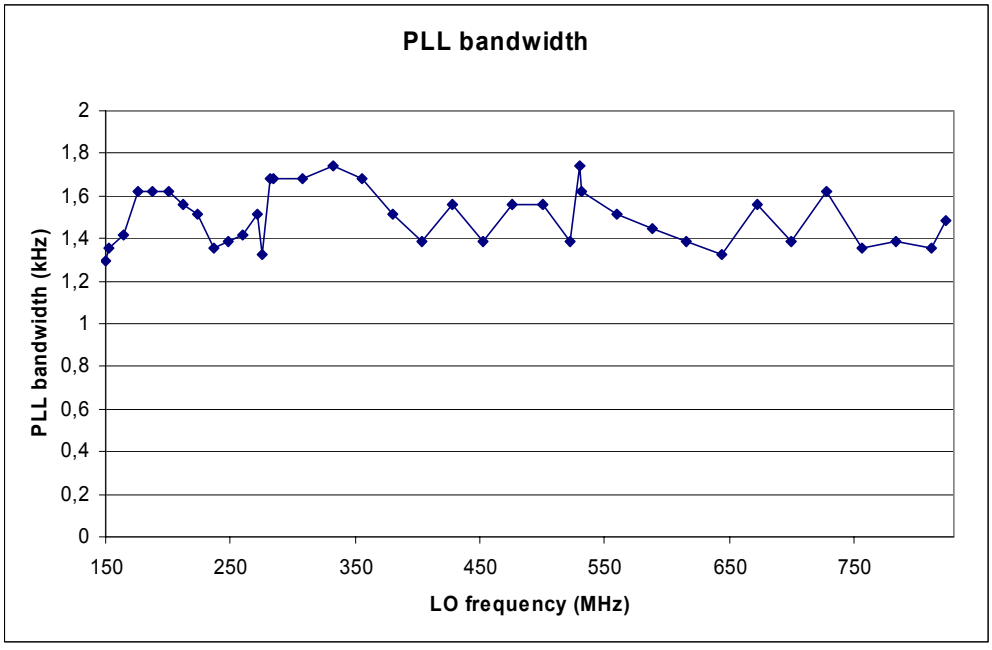


figure 36. PLL bandwidth in the conventional application (fstep=62.5kHz).

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 170	93 to 113	90
	170 to 218	113 to 161	60
	218 to 242	161 to 185	90
	242 to 254	185 to 197	130
	254 to 266	197 to 209	190
	266 to 276,143	209 to 219,143	280
MID	282 to 368	225 to 311	60
	368 to 440	311 to 383	90
	440 to 488	383 to 431	130
	488 to 522,143	431 to 465,143	280
HIGH	530 to 546	473 to 489	60
	546 to 686	489 to 629	90
	686 to 742	629 to 685	130
	742 to 770	685 to 713	190
	770 to 798	713 to 741	280
	798 to 824,143	741 to 767,143	410

Table 15. Charge-pump current programming for the 1MHz comparison frequency in the conventional hybrid application.

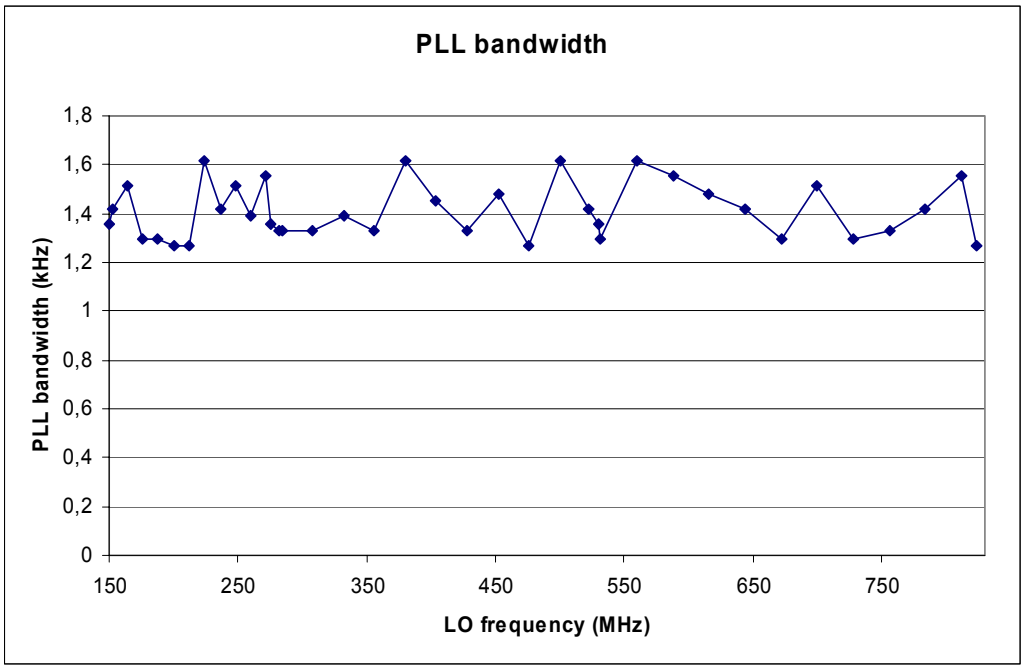


figure 37. PLL bandwidth in the conventional application (fstep=50kHz).

3.3.2.2 Switched concept

The loop filter design constraints for analogue and digital reception are opposite, consequently, if the same loop filter is shared for both applications, a trade off has to be found. In practice, the previous conventional loop filter has been determined first to cope with the interference rejections (analogue mode); thus, the phase noise characteristics are lower than the theoretical optimum performance. In order to improve the phase noise, the following concept splits the filtering characteristics of the filter.

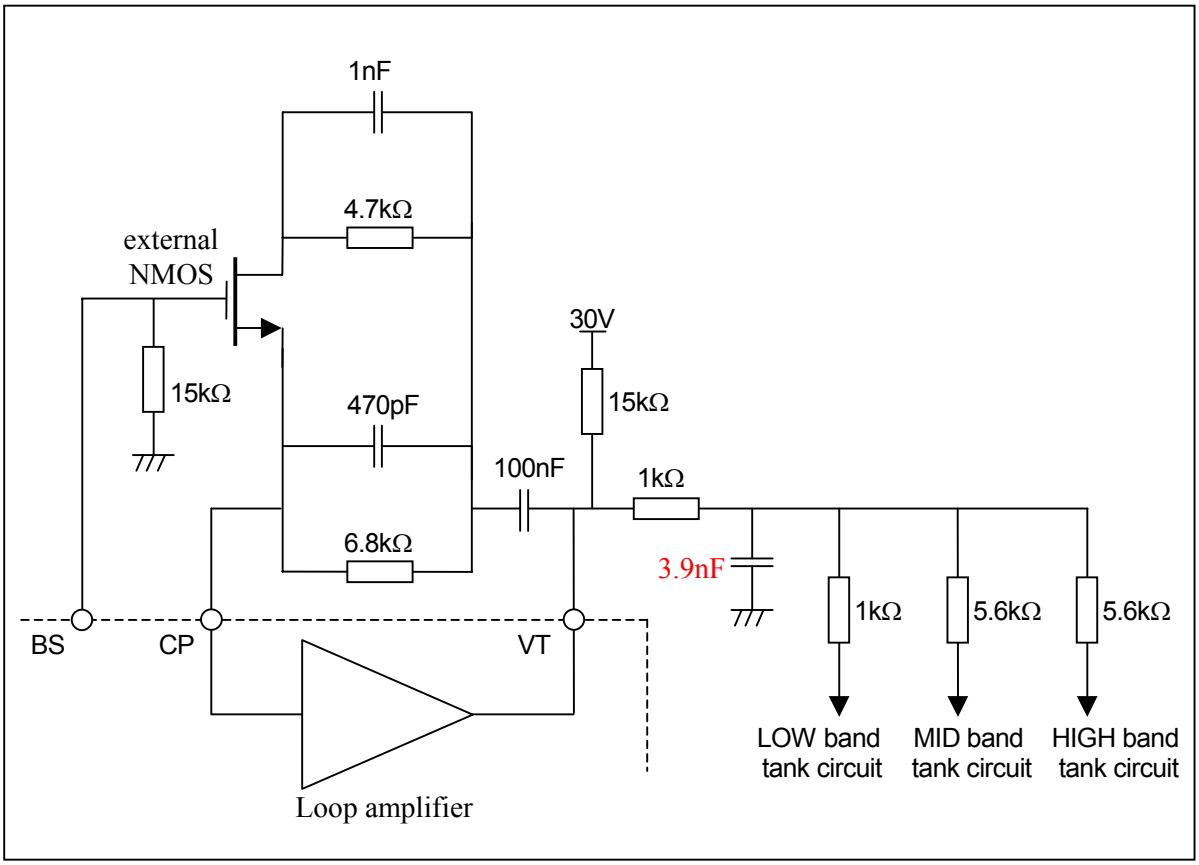


figure 38. Switched loop filter for digital and analogue reception (ISDB-T & NTSC Japan standards).

Note: the external transistor used in the switched loop filter is a BSH111 NMOS.

- **Switched concept principle**
  - In case of digital reception, the output port BS is programmed OFF, consequently, the external NMOS transistor is switched OFF: the gate voltage is 0V. Therefore the transistor presents a high impedance to the charge–pump output, the 4.7kΩ resistor and the 1nF capacitance are disconnected. The loop filter can be simplified as follows:

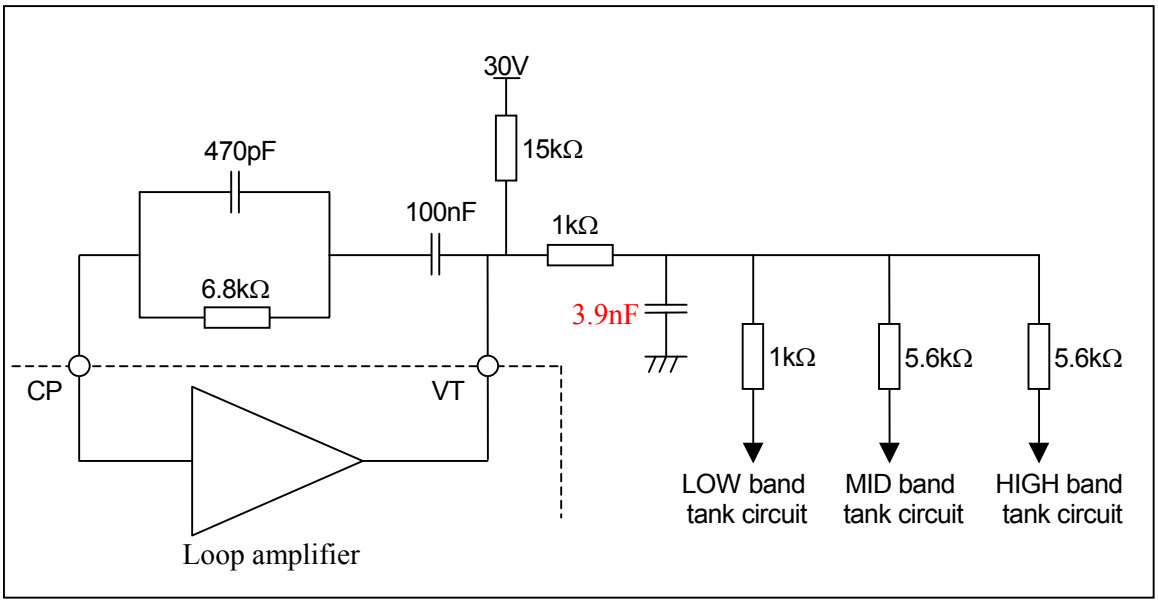


figure 39. Simplified view of the switched filter in case of digital reception.

- On the opposite, when receiving an analogue channel, BS is switched ON, thus the gate voltage is higher than 4.6V (5V – $V_{ds,sat}$). The NMOS is switched ON, and presents a low impedance $R_{ds,on}$, the 4.7kΩ resistor and the 1nF capacitance are connected in parallel with the 6.8kΩ resistor and the 470pF capacitance. The schematic can be simplified as follows:

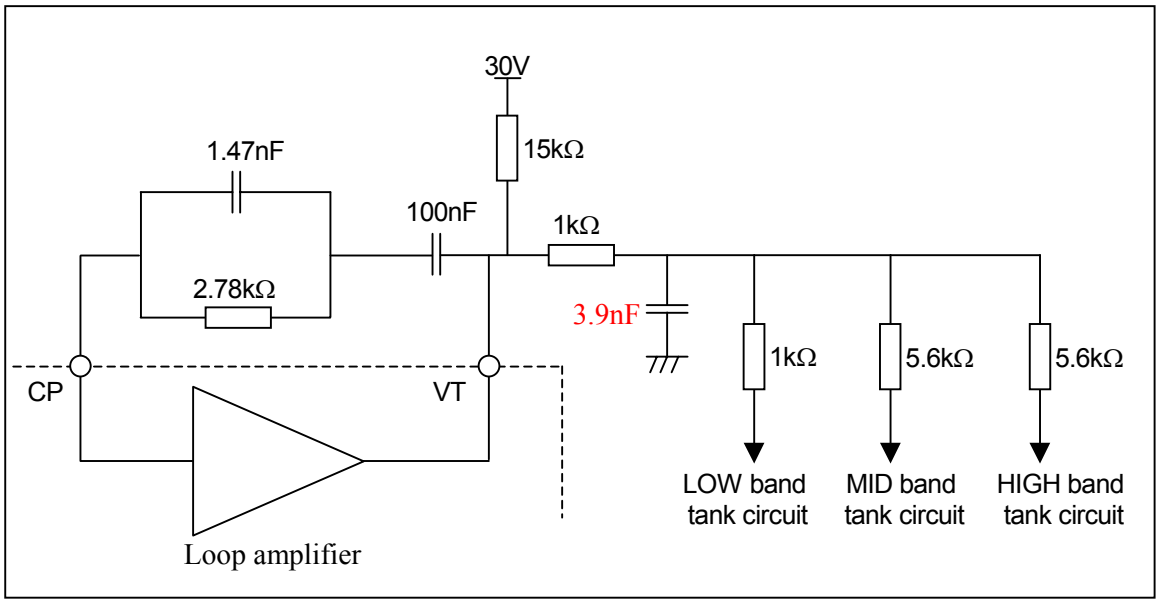


figure 40. Simplified view of the switched filter in case of analogue reception.

- **Digital reception with the switched filter.**

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 176	93 to 119	190
	176 to 236	119 to 179	130
	236 to 248	179 to 191	190
	248 to 260	191 to 203	280
	260 to 272	203 to 215	410
	272 to 276	215 to 219	600
MID	282 to 404	225 to 347	130
	404 to 452	347 to 395	190
	452 to 500	395 to 443	280
	500 to 510	443 to 453	410
	510 to 522	453 to 465	600
HIGH	530 to 588	473 to 531	130
	588 to 700	531 to 643	190
	700 to 756	643 to 699	280
	756 to 784	699 to 727	410
	784 to 824	727 to 767	600

Table 16. Charge-pump current programming for 4MHz comparison frequency in the switched application (ISDB-T standard).

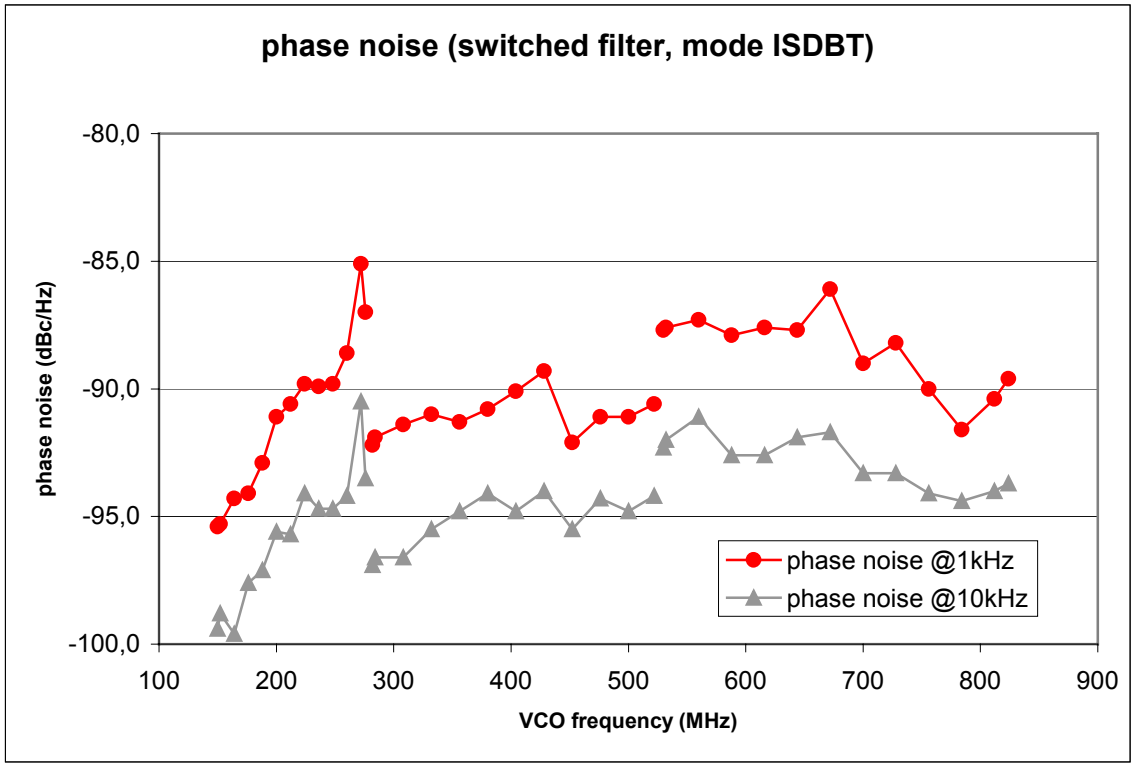


figure 41. Phase noise measurement in the switched application (ISDB-T).

- **Analogue reception with switched application**

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 272 272 to 276	91,25 to 213,25 213,25 to217,25	40,0 60,0
MID	282 to 500 500 to 522	223,25 to 441,25 441,25 to 463,25	40,0 60,0
HIGH	530 to 756 756 to 812 812 to 824	471,25 to 697,25 697,25 to 753,25 753,25 to 765,25	40,0 60,0 90,0

Table 17. Charge-pump current programming for the 2MHz comparison frequency in the switched application.

NB: The Table 17 is identical to the Table 14 (charge-pump current programming for the 2MHz comparison frequency in the conventional hybrid application).

band	osc (MHz)	RF (MHz)	charge pump current (uA)
LOW	150 to 260 260 to 272 272 to 276	91,25 to 201,25 201,25 to 213,25 213,25 to 217,25	40,0 60,0 90,0
MID	282 to 476 476 to 500 500 to 522	223,25 to 417,25 417,25 to 441,25 441,25 to 463,25	40,0 60,0 90,0
HIGH	530 to 728 728 to 756 756 to 812 812 to 824	471,25 to 669,25 669,25 to 697,25 697,25 to 753,25 753,25 to 765,25	40,0 60,0 90,0 130,0

Table 18. Charge-pump current programming for the 1MHz comparison frequency in the switched application.

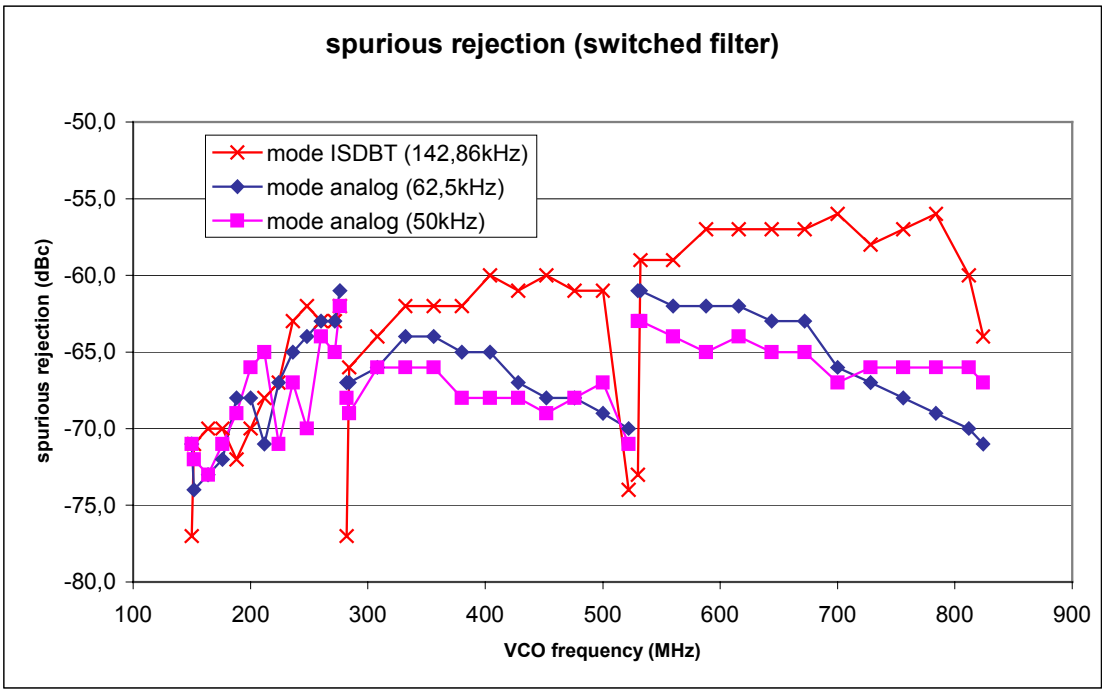


figure 42. Spurious rejection measurement in the switched application.

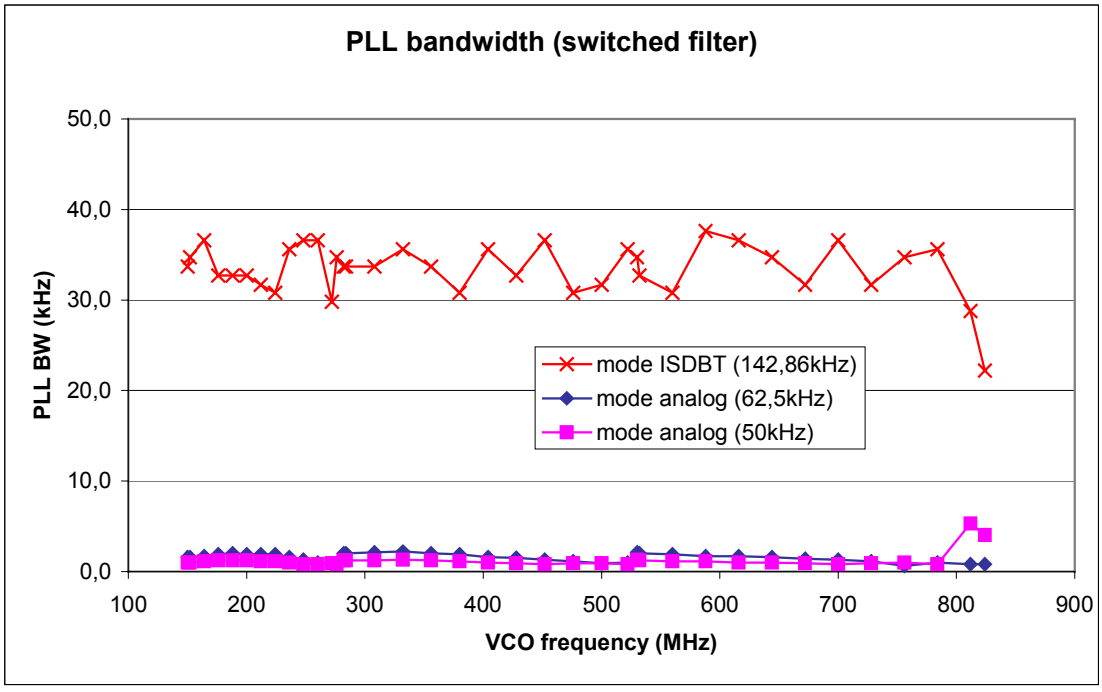


figure 43. PLL bandwidth in the switched application.

3.4 ALBC in TDA6650/51TT

Usually, the frequency step is determined by the standard, and can not be modified. In practice, a charge pump current table is associated with the loop filter design to fit with the VCO phase noise performances. In that way, the PLL loop bandwidth is optimized regarding the integrated phase jitter. For conventional circuits, it requires for each VCO frequency to program the divider ratios, the selected band and the best charge pump current.

The TDA6650/51TT includes the ALBC feature that simplifies the use of the integrated circuit. This function sets automatically the band and the charge pump current, it only requires for each VCO frequency to program the dividers ratios (main divider and reference divider) and the AGC take-over point level**.** There is no need to know which charge pump current is required to reach the best performance, the IC chooses the right current and the right band for each programmed VCO frequency.

I^2C programming without ALBC:

Start . Address byte . divider byte 1 . divider byte 2 . control byte 1 . band switch byte . control byte 2 . Stop

I^2C programming with ALBC :

Start . Address byte . divider byte 1 . divider byte 2 . control byte 1 . control byte 2 . Stop

NB: the “control byte 1” programs the reference divider ratio.
the “control byte 2” programs the AGC take-over point level.

The ALBC feature is activated or deactivated by programming T2.T1.T0 to 0.1.1.
When ALBC is activated, the charge pump current and the output ports are no more programmed by the corresponding bits in the I^2C programming, but are set according to the Table 19.

NB: the table 19 is in practice identical to the Table 4 (charge-pump current programming for the 4MHz comparison frequency in the digital application (DVB-T standard)). This means the ALBC feature is optimized for the associated application (figure 8).

NB: In this table, the PMOS output port BS3 is systematically associated to the High band.

band	osc (MHz)	RF (MHz)	charge pump current (uA)	PMOS output ports	band
	80 to 92	44 to 56	60	BS1 on, other ports off	LOW
	92 to 144	56 to 108	90	"	"
	144 to 156	108 to 120	130	"	"
	156 to 176	120 to 140	190	"	"
	176 to 184	140 to 148	280	"	"
LOW	184 to 193	148 to 157	410	"	"
	196 to 224	160 to 188	60	BS2 on, other ports off	MID
	224 to 296	188 to 260	90	"	"
	296 to 380	260 to 344	130	"	"
	380 to 404	344 to 368	190	"	"
	404 to 448	368 to 412	280	"	"
	448 to 472	412 to 436	410	"	"
MID	472 to 479	436 to 443	600	"	"
	484 to 604	448 to 568	130	BS3 on, other ports off	HIGH
	604 to 676	568 to 640	190	"	"
	676 to 752	640 to 716	280	"	"
	752 to 868	716 to 832	410	"	"
HIGH	868 to 900	832 to 864	600	"	"

Table 19. Charge pump current and output ports when ALBC is activated.

4 WIDE BAND AGC

4.1 Wide band AGC function

"Wide band AGC" means that the AGC level detector operates on a large input frequency bandwidth. It is therefore sensitive to the strong neighboring channels as can be met in digital applications. On the contrary, classical AGC detector operates after a SAW filter (narrow band). The narrow band system cannot handle high adjacent channels as it is not able to detect the real power available at the IF amplifier output. It cannot prevent this amplifier from saturation in that case.
Wide band AGC detects the strong neighboring channel and lower the RF gain to prevent saturation of the IF amplifier.

4.2 Normal / fast mode

AGC response time must be as quick as possible when a new channel is selected. Once correct gain is set, AGC response time must be slow enough to avoid any "demodulation" of the signal. TDA6650/51 offers 2 AGC currents to cope with the 2 requirements.
Fast mode is recommended when a new channel is selected. It enables to adjust gain in 58ms or less. After that period, normal AGC mode must be selected.
As explained in paragraph 4.6.5, the current setting changes the cutoff frequency of the AGC loop. With Iagc=9µA, loop is able to respond with several kHz bandwidth, it can lead to a demodulation of the input carrier or to a fast gain variation. This may disturb reception of the wanted channel.

4.3 Wide band AGC overview

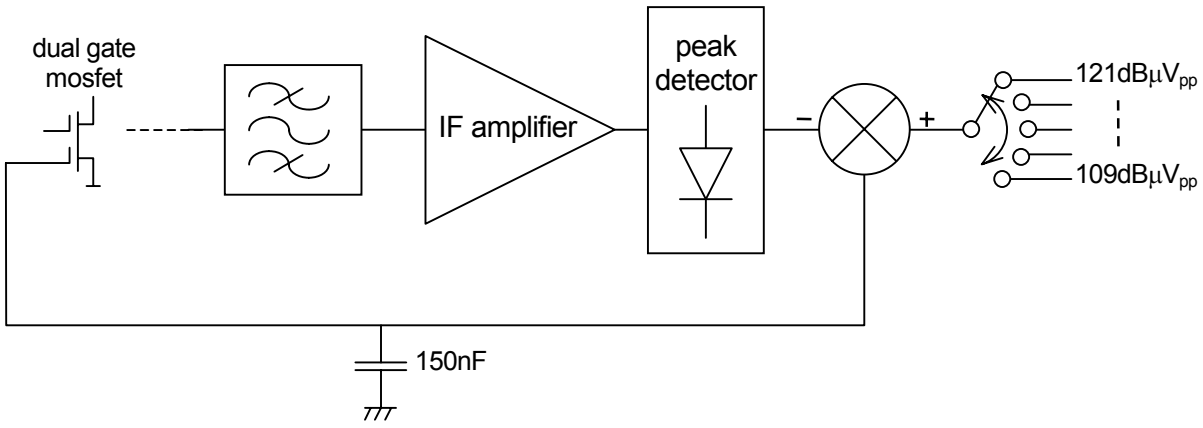


figure 44. AGC Loop

The AGC output delivers a current that depends on the IF output voltage amplitude and of the TOP value programmed via the I^2C bus. The output current, I_{agc}, is integrated by a capacitor (150nF typical). The resulting voltage enables to adjust the gain of a dual gate MOSFET.

NB: It is possible to switch AGC detector OFF, then AGC output is in high impedance state (I_{agc} current = 0).

4.4 wide band agc block diagram

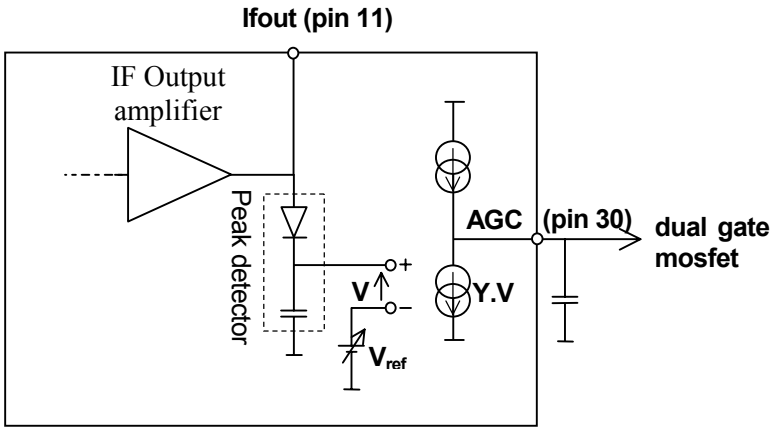


figure 45. TDA6651TT Wide band AGC block diagram

- The level detection is performed thanks to a standard peak detector.
- The detected level is compared to a selectable reference (V_{ref}). Each Take Over Point (TOP) corresponds to a reference level V_{ref}.
- The AGC output is a current type output, built with 2 current sources:

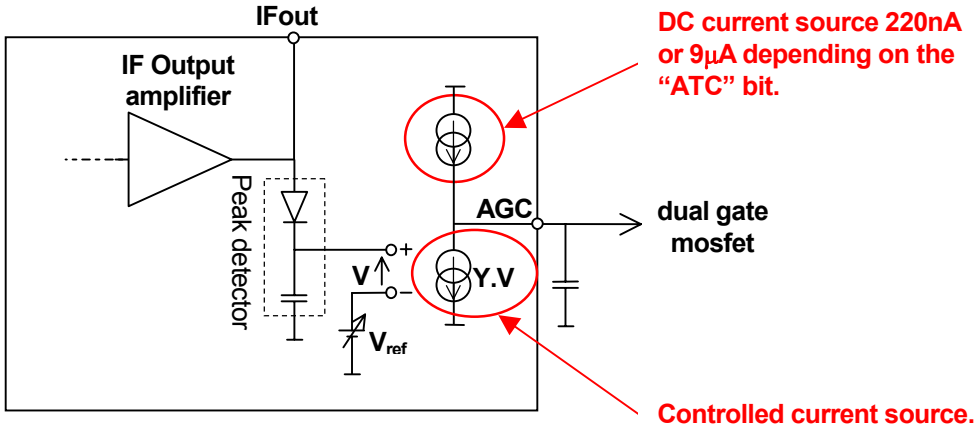


figure 46. AGC current sources.

- The DC current source is active for all AGC modes (excepted for "I_{agc}=0" mode AL2.AL1.AL0=1.1.0).
- The controlled current source sinks a current from 0 to 400µA depending on the level detected.

- When the wide band AGC loop is closed, **at the operating point**, the sum of the 2 currents is null. The loaded capacitor fixes the AGC voltage.

4.5 transient behavior

In practice, 2 transient behaviors may occur. One due to a rising IF amplitude, the other due to a falling amplitude. The time constants are different simply because the 2 current sources do not have the same value (220nA versus 400μA_{max}).

The TDA6650/51TT datasheet mentions a time constant corresponding to a falling edge, with the complete AGC voltage excursion (worst case). (equivalent to the full AGC range).

$$T = C \times \frac{\Delta V}{I_{agc}}$$

with T the time constant, C the capacitor value, ΔV the AGC voltage excursion and I_{agc} the wide band detector output current.

In the worst case :

- I_{agc} = 220nA (bit ATC = 0)
- ΔV = 3V (full excursion needed to get the full AGC range)
- C = 150nF

$$\Rightarrow \mathbf{T \approx 2s}$$

NB: If I_{agc} = 9μA_{max} (bit ATC = 1), T ≈ 50ms with the same hypothesis.

In case of a smaller step, the time constant is of course reduced.

4.6 small signal behavior

The wide band AGC loop can be modeled to analyze the small signal behavior.

4.6.1 Loop parameters

Loop is composed of three parts:
- The dual gate MOSFET,
- The voltage detector,
- The integration capacitor.

For each part, a gain can be expressed. The product of the 3 gains gives the total loop gain and therefore the cut off frequency of the loop.

4.6.2 MOSFET gain

Regarding the AGC loop, the MOSFET gain is the ratio of RF gain variation to V_{GS} voltage variation.
Typically, for BF904, gain is: 1dB/V<MOSFET Gain<35dB/V

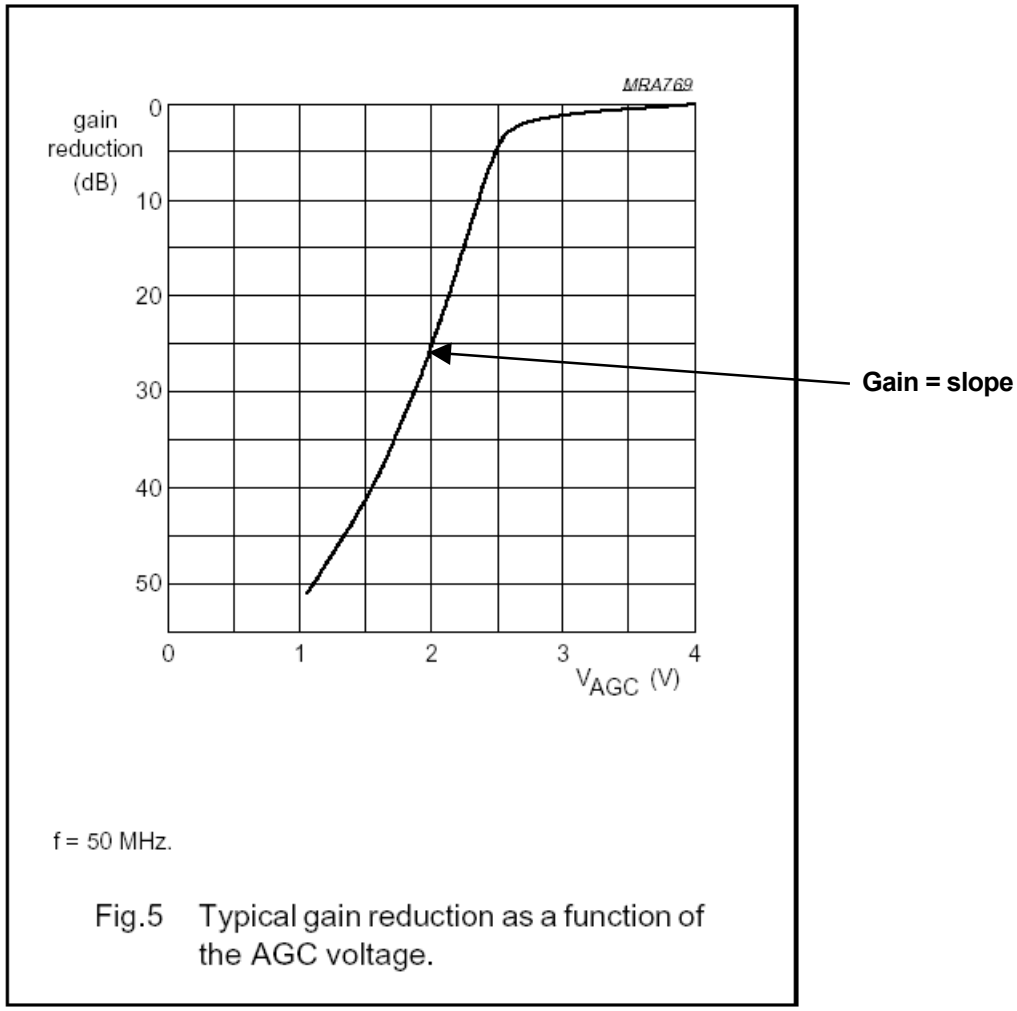


Fig.5 Typical gain reduction as a function of the AGC voltage.

figure 47. BF904 mosfet gain

4.6.3 Voltage detector gain

The small signal transfer function of the AGC detector is obtained thanks to a measurement of the MOPLL characteristic: AGC (pin 30) output current as a function of the MOPLL input or output level.

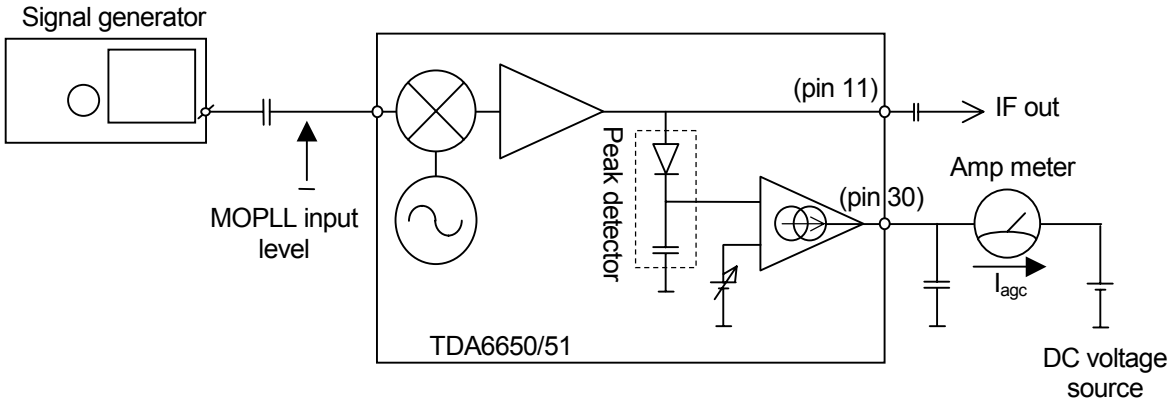


figure 48. Measurement set up of the AGC detector characteristic.

figure 49 & figure 50 gives the typical characteristic of I_{agc} versus $V_{IF\ out}$ (MOPLL IF output voltage measured with a sine-wave carrier at the input of the MOPLL) in AGC slow or fast mode for the different Take Over Points.

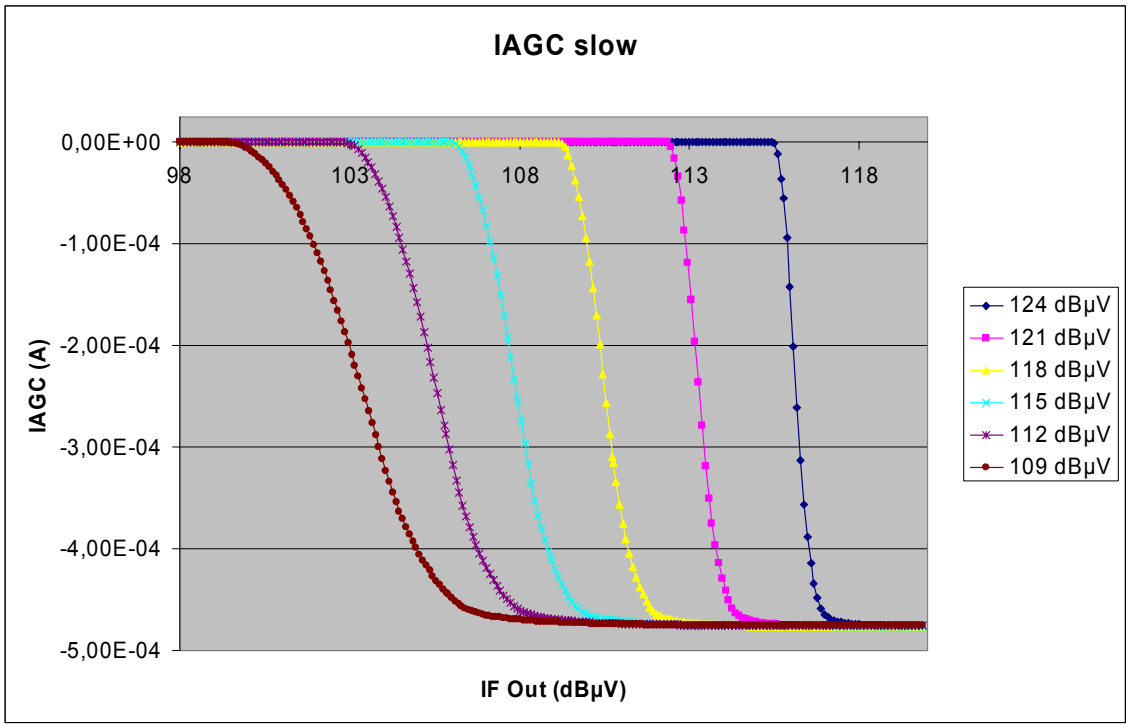


figure 49. I_{agc} versus $V_{IF\ out}$ (slow AGC mode)

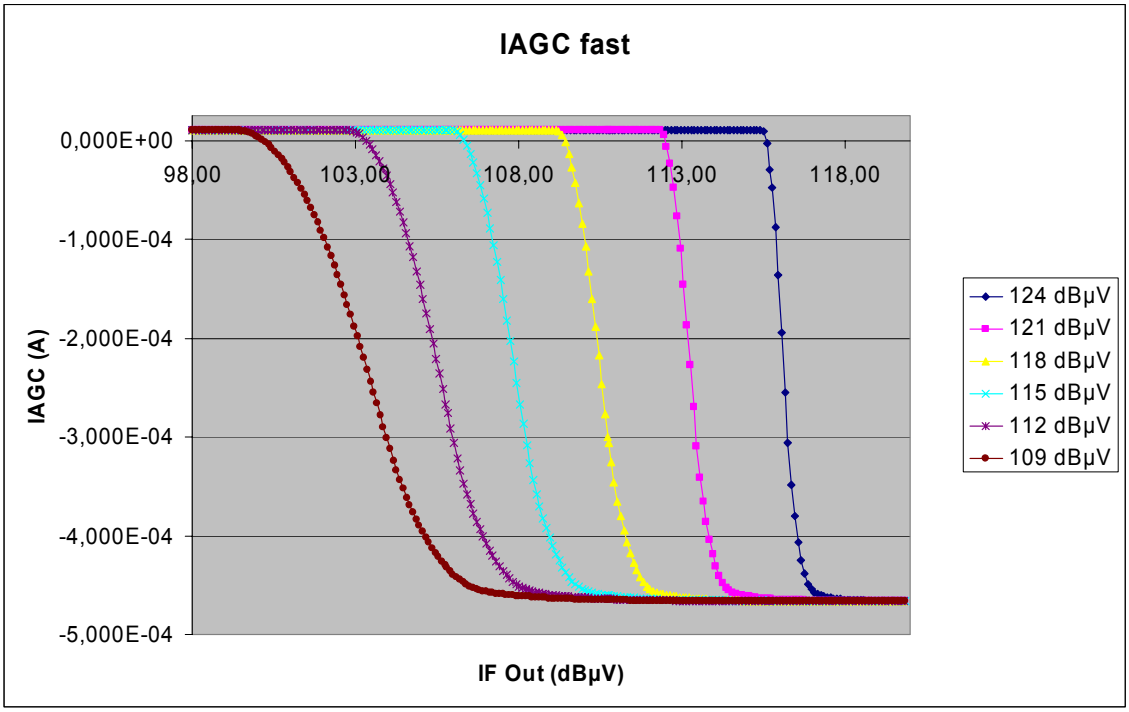


figure 50. I_{agc} versus $V_{IF\ out}$ (fast AGC mode)

(equation 4.)

$$Detector\ gain = \frac{\Delta I_{agc}}{\Delta V_{outIF}}$$

at the operating point (⇔ *slope at I_{agc} = 0.)*

It can be found from figure 49 & figure 50 for each curve:
For slow AGC mode (ATC=0) Detector gain ≤ 10µA/dB
For fast AGC mode (ATC=1) Detector gain ≤ 102µA/dB.

The highest slopes (maximum detector gain) are measured with the TOP 124dBµVpp.

NB: in a previous document (CC0309), 0.9µA/dB was given for the detector gain. It was an error.

4.6.4 Capacitor gain

(equation 5.)

$$Cgain = \frac{\Delta V}{\Delta I} = \frac{1}{C \times p}$$

4.6.5 Loop response

The AGC closed loop transfer can be defined as:

(equation 6.)

$$\frac{Out}{In} = \frac{MOSFET\ gain \times Detector\ gain \times \frac{1}{C \times p}}{1 + (MOSFET\ gain \times Detector\ gain \times \frac{1}{C \times p})} = \frac{1}{1 + \mathrm{T} \times p}$$

$$\text{With } \mathrm{T} = \frac{C}{MOSFET\ gain \times Detector\ gain}$$

The loop acts as a first order low pass filter with cut off frequency dependant of C capacitance value, MOSFET gain and detector gain.

$$f_{cutoff} = \frac{MOSFET\ gain \times Detector\ gain}{C \times 2\pi}$$

This is valid as long as the detector is used near balance (I_{agc}=0). This corresponds to signal with slowly varying amplitude.

In case normal AGC is selected, TOP 124dBµVpp, typical values are :
- MOSFET gain = 35dB/V
- Detector gain = 10µA/dB
- C = 150nF
- **f_{cutoff} = 370Hz**
-

In case fast AGC is selected, typical values are:
- MOSFET gain = 35dB/V
- Detector gain = 102µA/dB
- C = 150nF
- **f_{cutoff} = 3.8kHz**
-

4.6.6 influence of the cut off frequency

In case of the reception of an AM modulated signal, the AGC voltage will follow the modulation for frequencies up to the AGC loop cut off frequency. Therefore, the cut off frequency must be low enough to ensure constant AGC voltage.

4.7 AGC loop stability

4.7.1 Simple AGC configuration

The simplest AGC connection uses only one external capacitor (150nF for example).

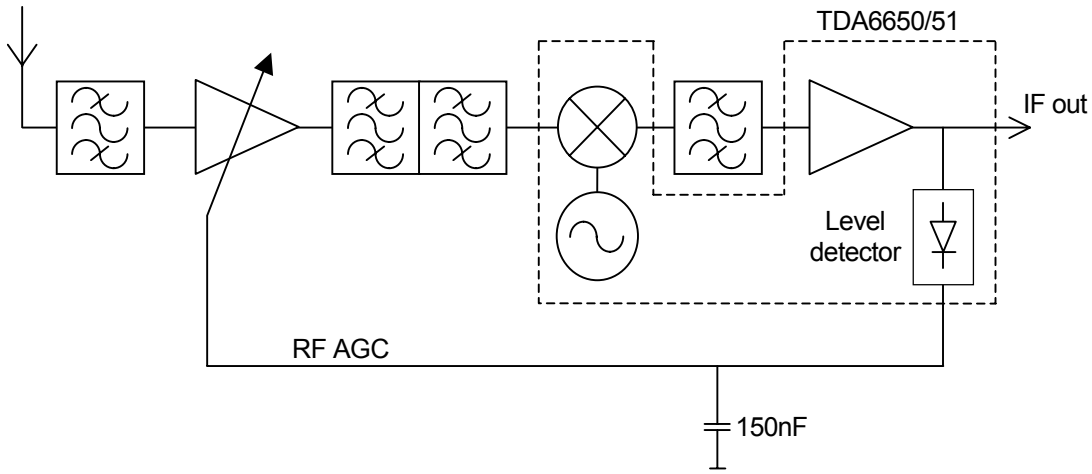


figure 51. Simple AGC configuration

The AGC loop behavior (stability) can be modeled for small signal analysis. The building blocks are:

- the dual gate mosfet
- the mopll agc detector
- the external capacitor

The open loop small signal analysis gives the loop phase margin and cut off frequency.

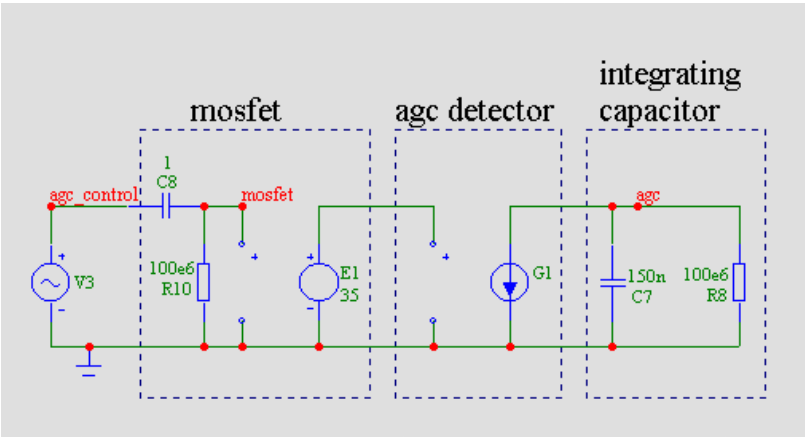


figure 52. Small signal model of the AGC loop (open loop)

NB: the very high resistors (100MΩ) have been included to avoid problems of simulation convergence.

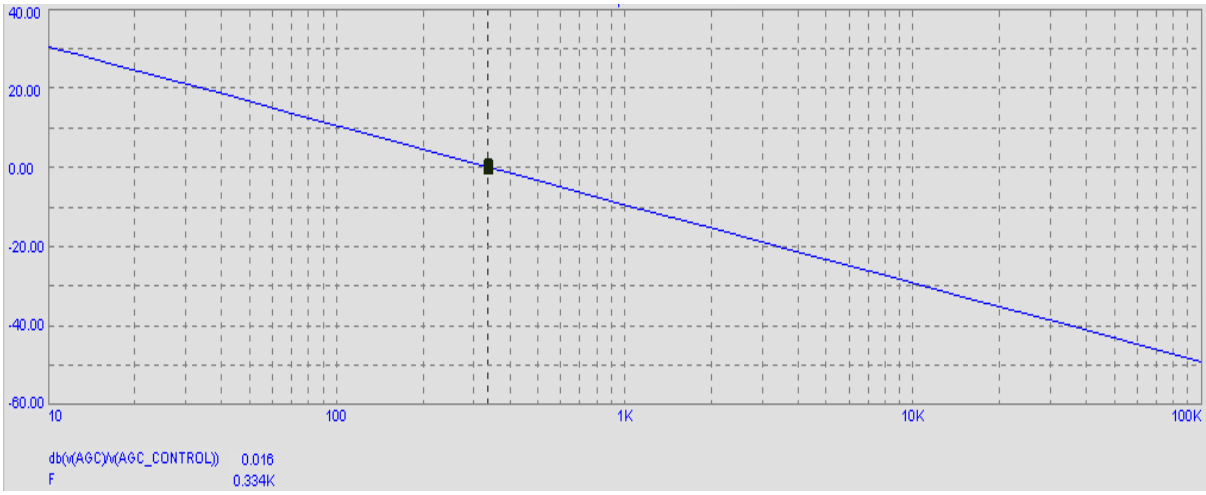


figure 53. Amplitude transfer dB(AGC / AGC_control)

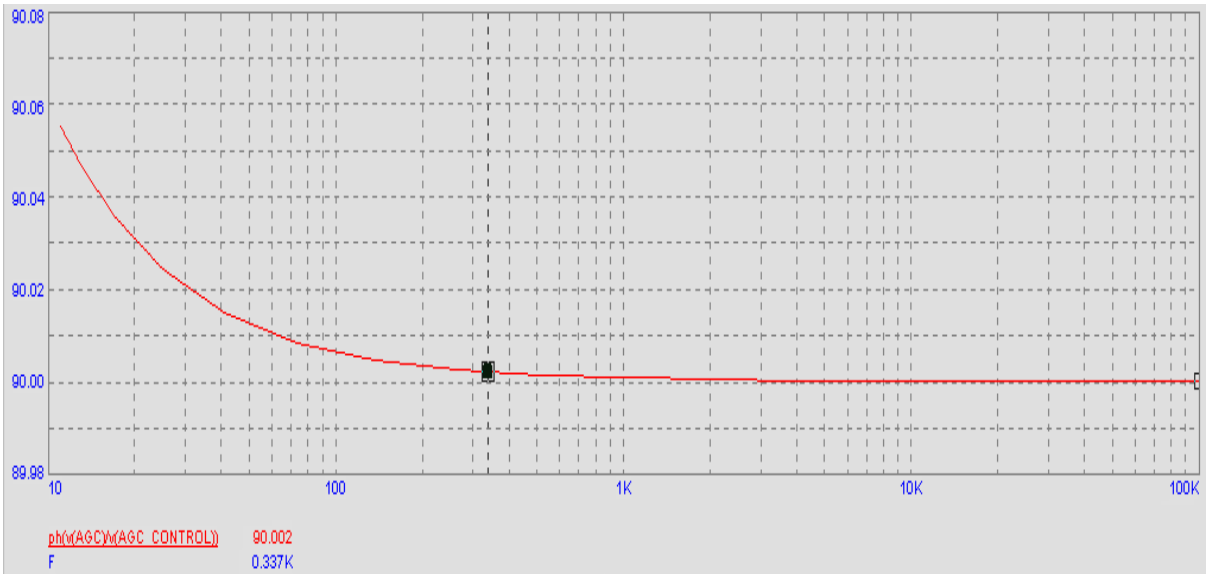


figure 54. Phase of the transfer ph(AGC / AGC_control)

AGC slow mode characteristics:

- Cut off frequency = 330Hz
- Phase margin = 90°

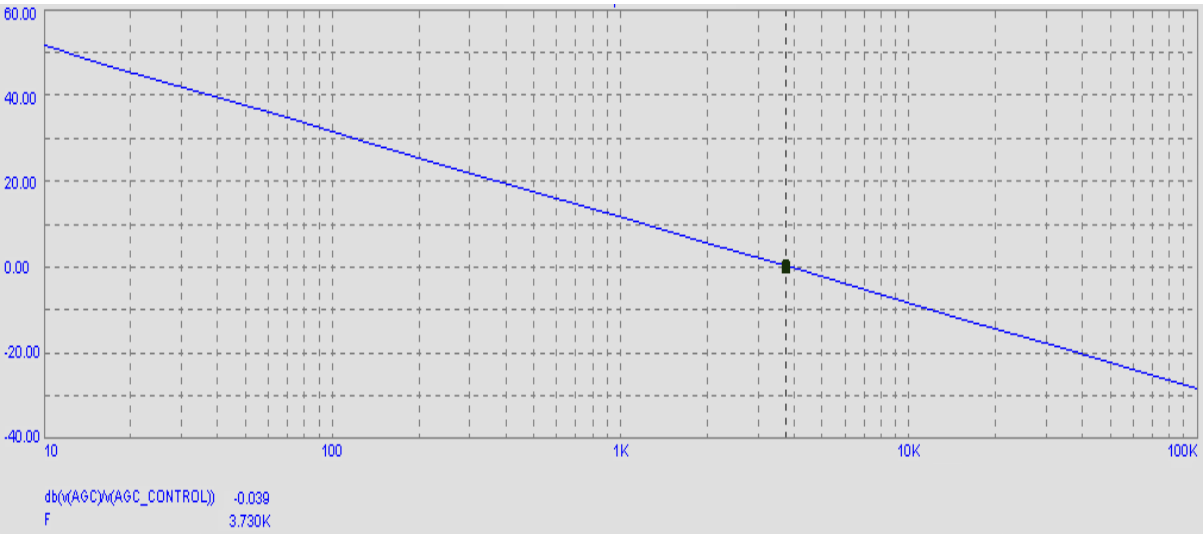


figure 55. Amplitude transfer dB(AGC / AGC_control)

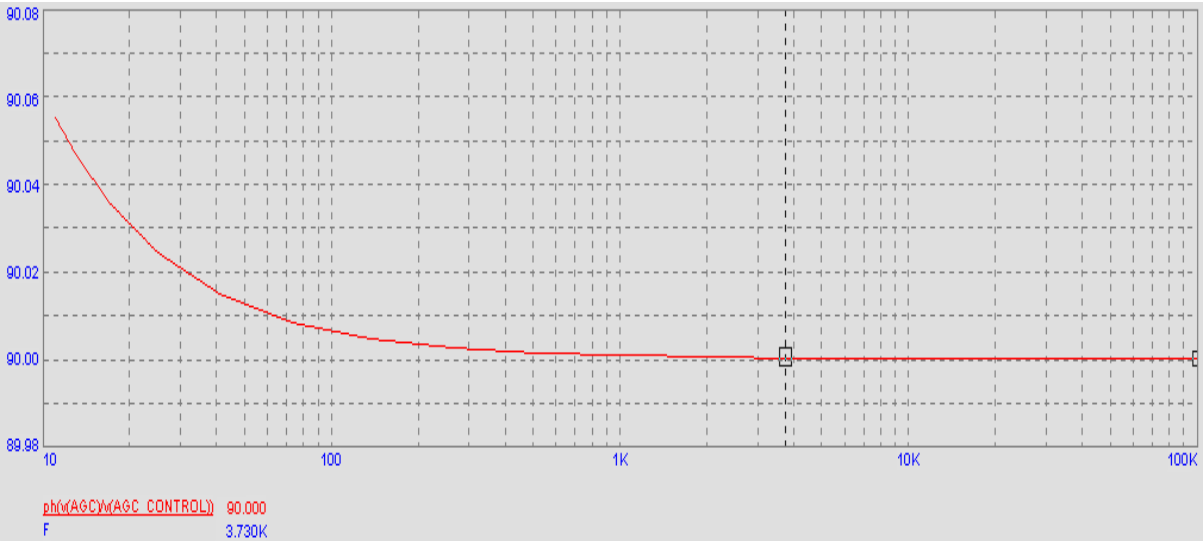


figure 56. Phase of the transfer ph(AGC / AGC_control)

AGC fast mode characteristics:

- Cut off frequency = 3.7kHz
- Phase margin = 90°

The loop is completely stable whatever the AGC mode (phase of the open loop transfer = 90°)

4.7.2 AGC loop including R-C poles

Usually, in tuners, R-C poles are included in the AGC path (for filtering purposes). The poles influence the loop response. If the R-C cut off frequency is low, the phase margin might be degraded.

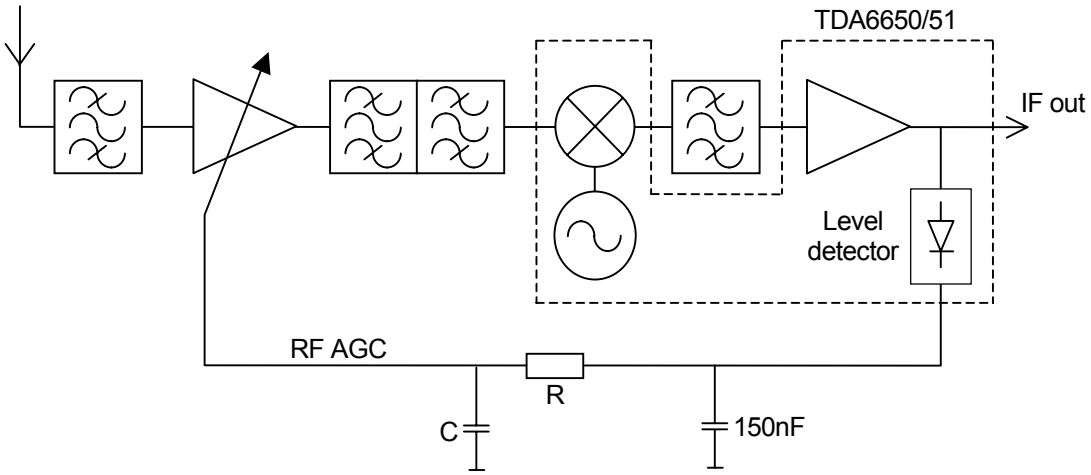


figure 57. AGC loop including a R-C pole.

For stability, the fast AGC mode might be critical : when the AGC detector gain is high, the AGC loop phase margin is reduced by a RC pole.

Example : R = 2.2kΩ,
C = 10nF

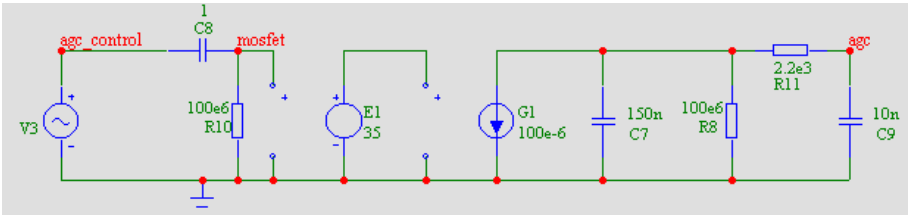


figure 58. Small signal model of the AGC loop with a R-C pole (open loop)

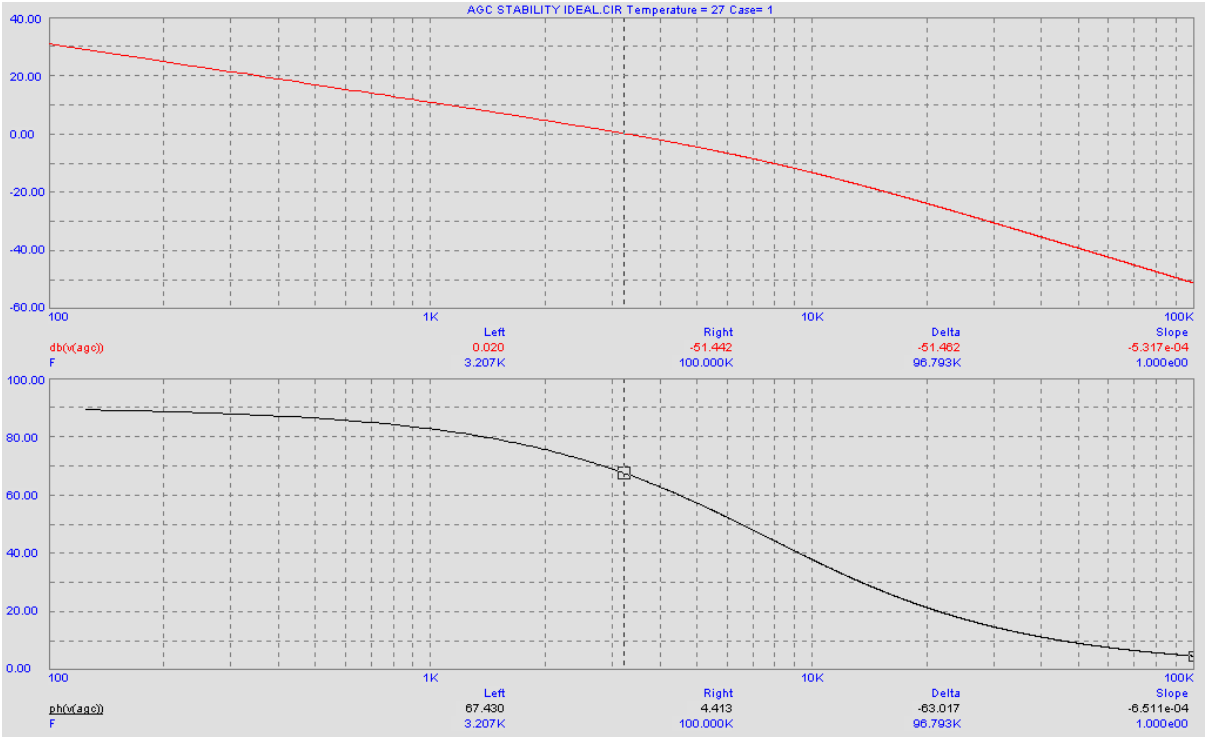


figure 59. Amplitude and phase transfer.

AGC fast mode characteristics with a R-C pole:

- R = 2.2kΩ & C = 10nF $\Rightarrow$ $f_{cut\ off\ RC}$ = 7.2kHz
- Cut off frequency = 3.2kHz
- Phase margin = 67.4°

The phase margin is reduced when introducing a R-C pole. It is advised to keep the phase margin higher than 40°.

4.7.3 Conclusions for the design of the AGC loop

The choice of the various element of the wide band AGC (current source of the level detector, external capacitor) determines the transient behavior and the cut off frequency of the loop :

1. The time constant linked to an amplitude step is longer for a step down.

→ 2 seconds for the full AGC range (C=150nF, Mosfet = BF904, I_{agc}=220nA).
→ 50ms for the full AGC range (I_{agc}=9µA).
Consequently when switching from one channel to another, it is better to select the “search” mode (I_{agc}=9µA) to speed up the AGC voltage transition.

2. When the channel is locked, it is preferable to set a low cut off frequency: the cut off frequency is below 500Hz in “normal” mode (2s , C=150nF, Mosfet = BF904, I_{agc}=220nA).

3. The various poles included in the AGC path must be designed carefully in order to keep a sufficient phase margin (40° minimum).

4.8 AGC output loading

For normal and proper operation of the AGC, nothing else than a capacitor and the MOSFET gates must be connected to the AGC pin. When AGC loop is closed, almost no dc current is sinking nor sourcing into or from the AGC pin.
In case an additional device is connected to AGC pin, 2 problems may arise:

- With a pull down resistor, the AGC output voltage is dropping because AGC output current cannot exceed 220nA in normal mode. It means **that the MOSFET cannot reach maximum gain**.
- With a pull up resistor, the detector characteristic is shifted, detector gain is increased and **the AGC loop cut off frequency is increased**.

For good operation, I_{agc} must be near zero when AGC loop is closed. Only high impedance can be connected to the AGC pin.

4.9 AGC detector limitations

The TDA6650/51 performances may be degraded within some specific conditions of use. This chapter describes the phenomenon and the conditions required to observe it: that degradation occurs when the local oscillator operates with a frequency close to an IF harmonic and when the AGC detector is activated. This chapter also indicates the critical RF frequencies for the standards PAL B, G, NTSC USA, and NTSC Japan.

4.9.1 failure description

The TDA6650/51TT demonstration board is used with the embedded wide band AGC detector according to the diagram described in figure 60. The TDA6650/51TT is programmed so as to deliver a fixed IF output (TOP level 109dBμV_{pp}, I_{agc}=220nA).

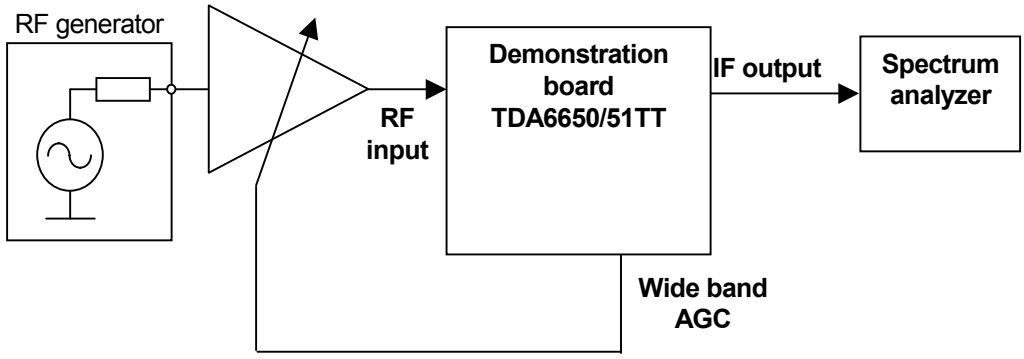


figure 60. Measurements diagram.

If the local oscillator frequency is close to an IF harmonic, the output spectrum is distorted (see figure 61), provided the AGC detector is active.

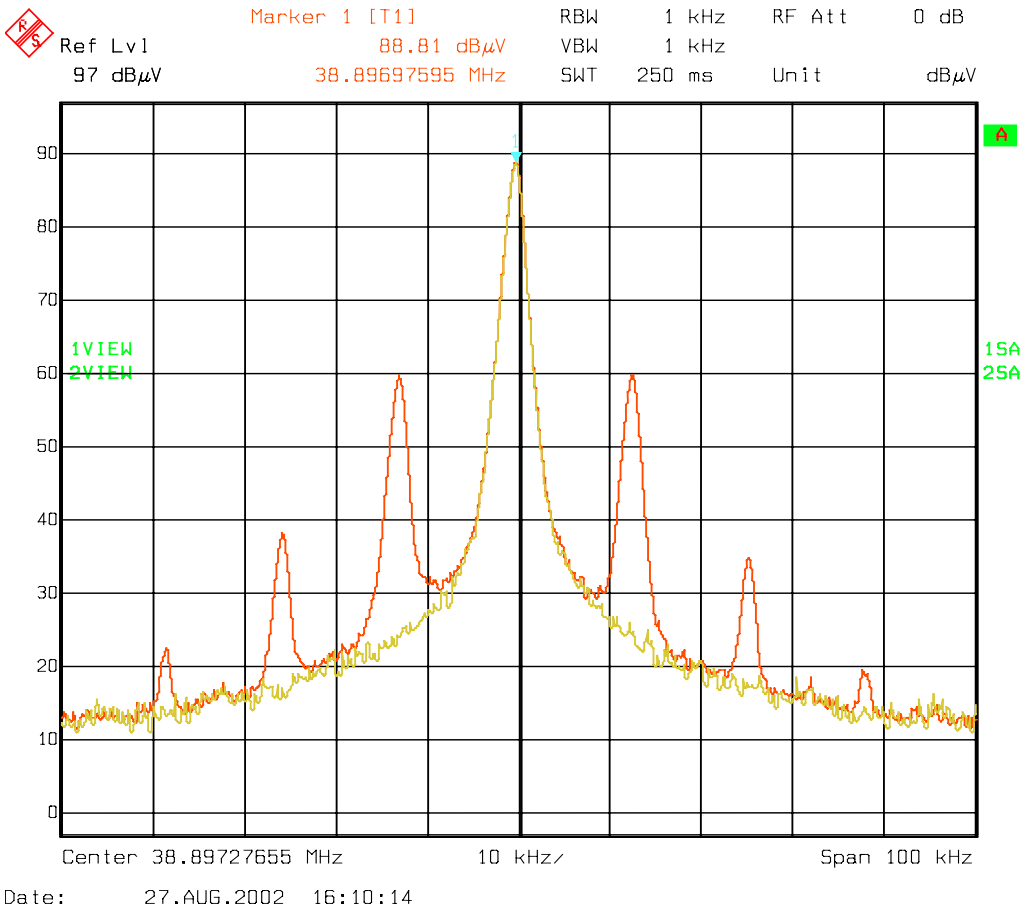


figure 61. Distortion of the IF output signal.

Measurement conditions:

- RF programmed 155.6MHz, IF 38.9MHz, I_{cp}=90µA, f_{step}=62.5kHz.
- Red curve: TOP 109dBµV_{pp}, I_{agc}=220nA.
- Yellow curve: I_{agc}=0.

4.9.2 Limitations in case of a 38.9MHz IF standard (Europe)

In case of PAL B, G standards, the vision output signal is programmed to 38.9MHz. The LO frequency is programmed within the range [87.15MHz , 894.15MHz]. The unwanted perturbation will occur in the 7 following configurations:

- LO frequency 3 = 3rd IF harmonic : 116.7MHz.
- LO frequency 4 = 4th IF harmonic : 155.6MHz.
- LO frequency 5 = 5th IF harmonic : 194.5MHz.
- LO frequency 6 = 6th IF harmonic : 233.4MHz.
- LO frequency 7 = 7th IF harmonic : 272.3MHz.
- LO frequency 8 = 8th IF harmonic : 311.2MHz.
- LO frequency 9 = 9th IF harmonic : 350.1MHz.

In practice, the perturbation becomes less critical when the LO frequency increases. The 10th harmonic does not introduce any visible perturbation.

The previous frequencies are not multiple of 62.5kHz (tuner frequency step), therefore they can not be synthesized, the practical synthesized frequencies are:

- LO frequency 3 = 116.6875MHz
- LO frequency 4 = 155.625MHz
- LO frequency 5 = 194.5MHz
- LO frequency 6 = 233.375MHz
- LO frequency 7 = 272.3125MHz
- LO frequency 8 = 311.1875MHz
- LO frequency 9 = 350.125MHz

The associated RF frequency is fed into the tuner input:

- RF frequency 3 = (LO frequency 3) × 2 ÷ 3 ≈ 77.792MHz
- RF frequency 4 = (LO frequency 4) × 3 ÷ 4 ≈ 116.719MHz
- RF frequency 5 = (LO frequency 5) × 4 ÷ 5 ≈ 155.6MHz
- RF frequency 6 = (LO frequency 6) × 5 ÷ 6 ≈ 194.479MHz
- RF frequency 7 = (LO frequency 7) × 6 ÷ 7 ≈ 233.411MHz
- RF frequency 8 = (LO frequency 8) × 7 ÷ 8 ≈ 272.289MHz
- RF frequency 9 = (LO frequency 9) × 8 ÷ 9 ≈ 311.222MHz

The degradation occurs not only for a precise RF frequency, but also within a range around the previous frequencies. It decreases when the RF signal is swept from the most critical frequency (-20dB/decade see figure 62).

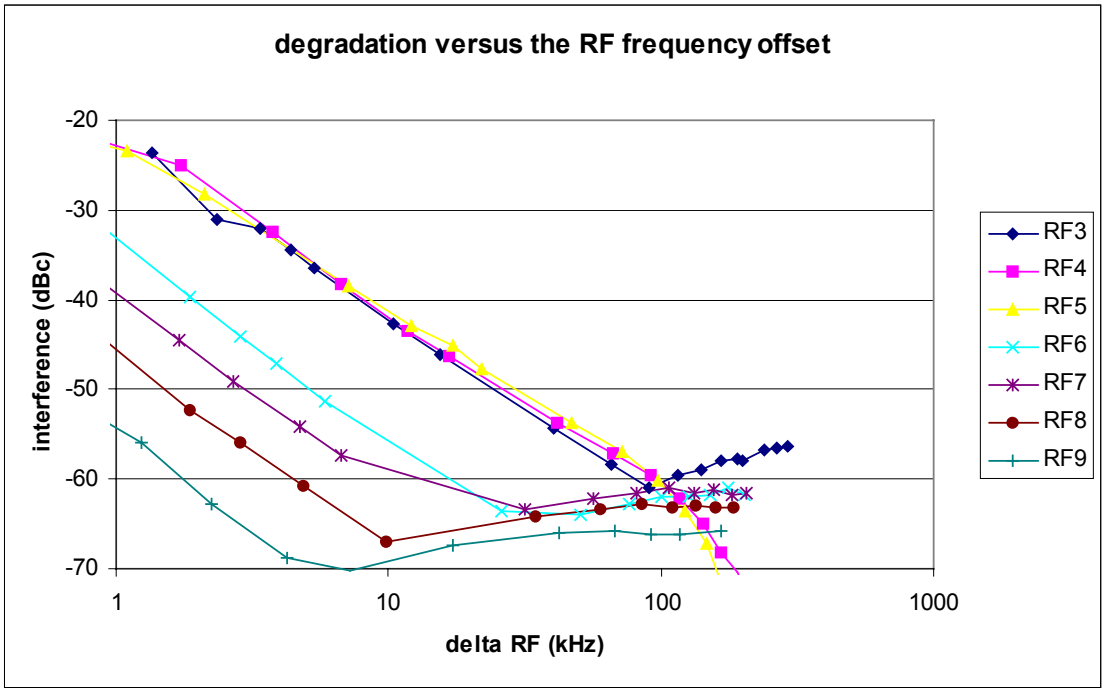


figure 62. Degradation measured at the IF output as a function of the RF offset.

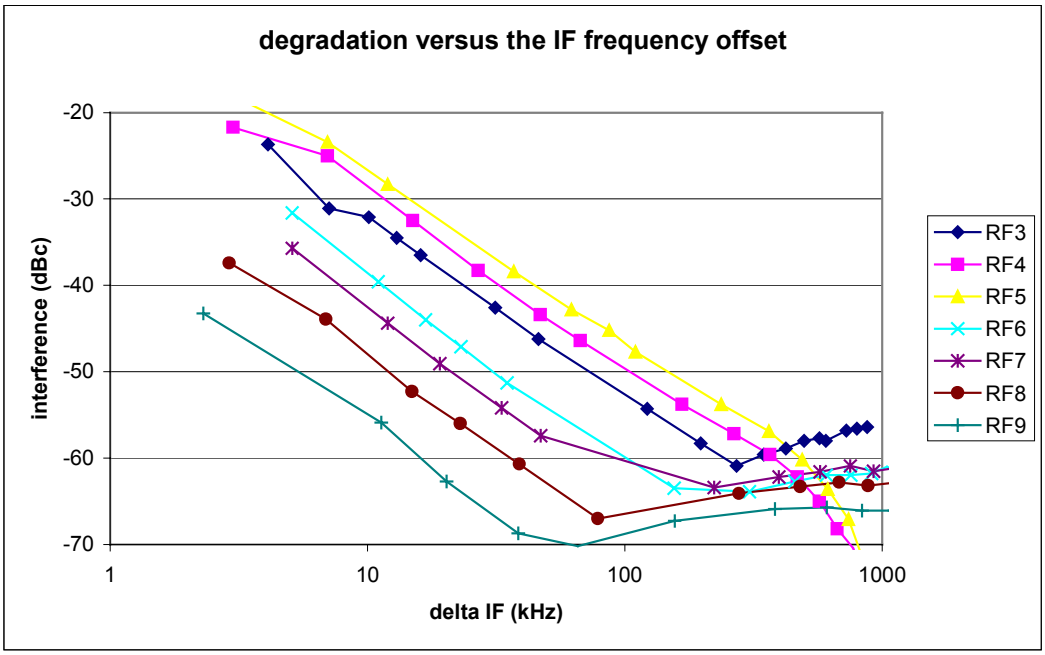


figure 63. Degradation measured at the IF output as a function of the IF offset.

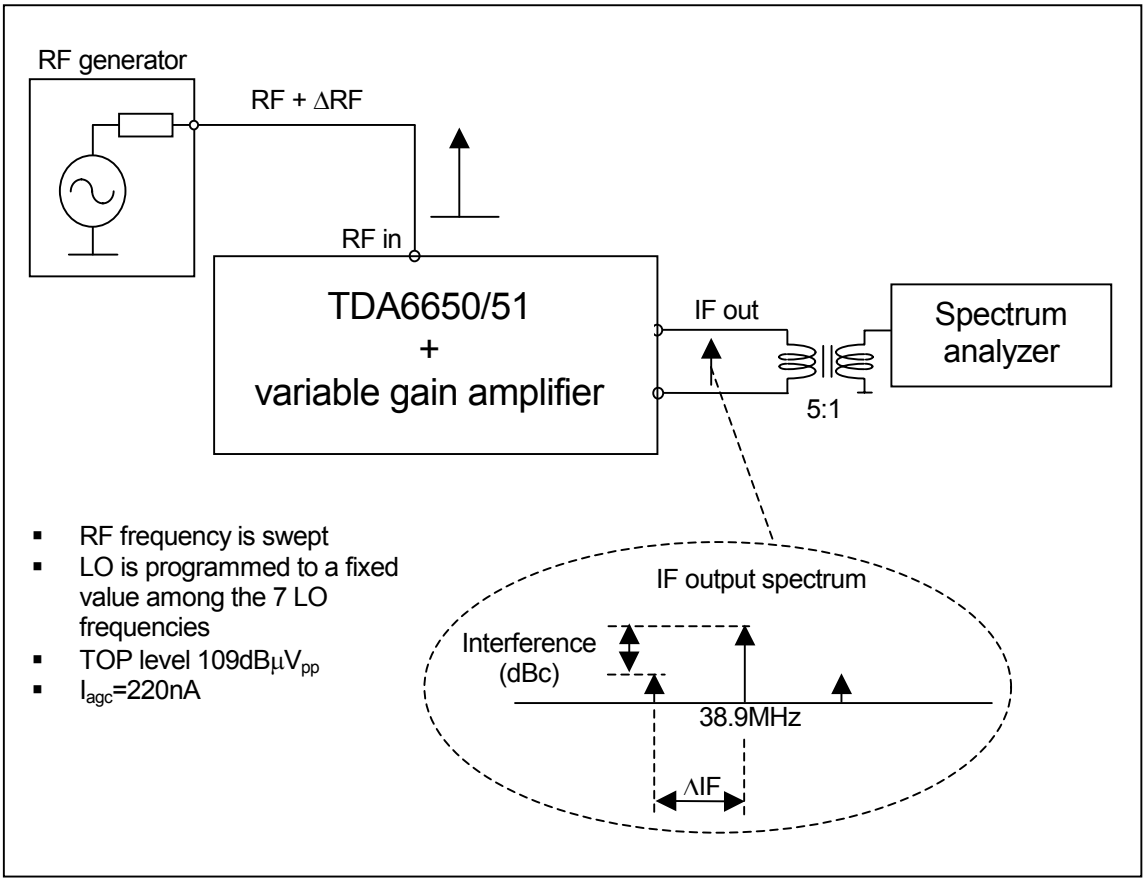


figure 64. Measurement set-up

NB: Depending on the 4MHz crystal accuracy, a few kHz tolerance must be taken into account for the LO frequencies.

The relation between the RF offset ΔRF and the interference offset measured at the IF output ΔIF is related in the figure 65.

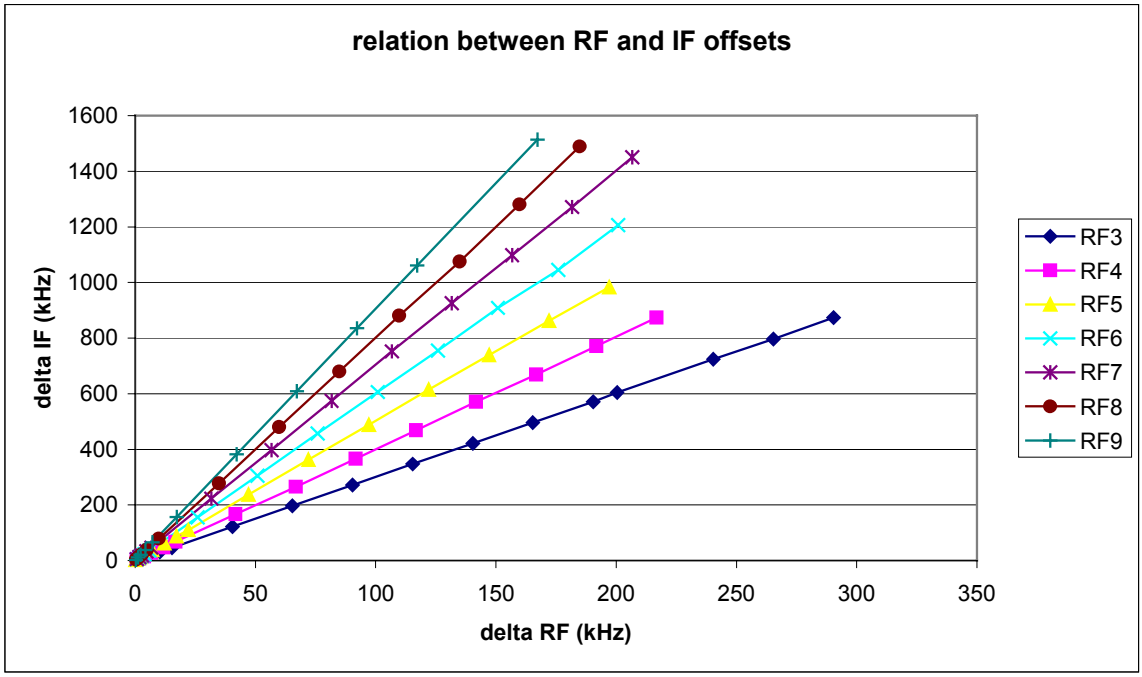


figure 65. ΔIF versus ΔRF.

Clearly, if "i" is the harmonic index, the relation between ΔIF and ΔRF is given by:

$$\Delta IF = i \times \Delta RF$$

(in case LO_i is programmed and (RF_i + ΔRF) is fed into the tuner input.)

For a 38.9MHz IF output standard, the 7 RF ranges cannot be used with the wide band AGC detector:

- 77.792MHz ± 100kHz ± 4MHz oscillator accuracy
- 116.719MHz ± 100kHz ± 4MHz oscillator accuracy
- 155.6MHz ± 100kHz ± 4MHz oscillator accuracy
- 194.479MHz ± 25kHz ± 4MHz oscillator accuracy
- 233.411MHz ± 10kHz ± 4MHz oscillator accuracy
- 272.289MHz ± 5kHz ± 4MHz oscillator accuracy
- 311.222MHz ± 2kHz ± 4MHz oscillator accuracy

NB: the degradation mechanism strongly looks like a pulling of the local oscillator (to be confirmed).

4.9.3 Limitations in case of a 45.75MHz IF standard (USA)

The critical RF frequencies are:

- RF frequency 3 = 91.5MHz
- RF frequency 4 = 137.25MHz
- RF frequency 5 = 183MHz
- RF frequency 6 = 228.75MHz
- RF frequency 7 = 274.5MHz
- RF frequency 8 = 320.25MHz

4.9.4 Limitations in case of a 58.75MHz IF standard (JAPAN)

The critical RF frequencies are:

- RF frequency 3 = 117.5MHz
- RF frequency 4 = 176.25MHz
- RF frequency 5 = 235MHz
- RF frequency 6 = 293.75MHz

4.9.5 conclusion

- The local oscillator behavior may be affected by the wide band AGC detector operation. The degradation occurs when the LO frequency is a multiple of the peak detector operating frequency (IF frequency).
- The degradation appears within precise RF input frequency ranges that do not correspond to any known analogue channel (PAL B, G; NTSC M; JAPAN M). This information has to be checked and agreed with the customer.

5 THERMAL CONSIDERATIONS

The junction temperature strongly influences the reliability of an IC. It must never exceed +150°C in any case. The PCB used in the application contributes in a large part to the overall thermal characteristic, therefore it must be designed to cope with the thermal requirements.

5.1 Junction temperature evaluation

The junction temperature can be evaluated knowing the thermal resistance between the junction and the ambient environment, the ambient temperature and the power dissipated in the IC.

5.1.1 Power dissipated in the IC

The power dissipated in the IC is split into 3 parts:

- The power P_1 consumed under VCC (VCCA and VCCD IC supply voltages).
- The power P_2 consumed in the output ports.
- The power P_3 consumed under the "33V" supply voltage.

(equation 7.) $$P_1 = V_{CC} \times I_{CC}$$

with I_{CC} supply current (excepted the current flowing into the output ports).

(equation 8.) $$P_2 = I_{output\ ports} \times V_{DSsat}$$

with V_{Dssat} output saturation voltage of the PMOS port.

(equation 9.) $$P_3 = V_t \times I_{high\ voltage\ transistor}$$

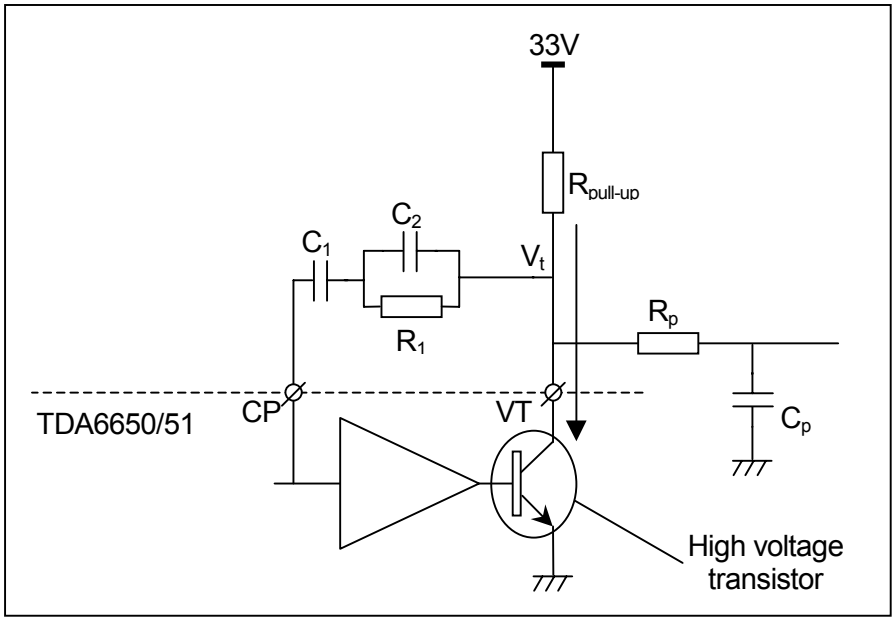


figure 66. Consumption in the high voltage transistor.

The total power P_{tot} dissipated in the IC is deduced from (equation 7.), (equation 8.) & (equation 9.):

(equation 10.)

$$P_{tot} = V_{CC} \times I_{CC} + V_{DSsat} \times I_{output\ ports} + V_t \times I_{high\ voltage\ transistor}$$

The maximum power is:

(equation 11.)

$$P_{tot\,\max} = V_{CC\,\max} \times I_{CC\,\max} + V_{DSsat\,\max} \times I_{output\ ports\,\max} + \left(\frac{33V}{2}\right)^2 \times \frac{1}{R_{pull-up}}$$

5.1.2 thermal resistance between junction and ambient environment

The thermal resistance strongly depends on the PCB layout characteristics:
- number of layers
- area of copper
- size of the PCB
- …

The thermal resistance can be evaluated through the measurement of a diode characteristic. Practical figures of the demonstration boards (PCB827-3 & PCB827-4) are given below:

$R_{th\ j\text{-}a}$ (°C/W)	board	Layer quantity	Type
96.5	PCB827-3	1	TDA6651TT
100.3	PCB827-4	1	TDA6650TT

5.1.3 junction temperature

The elevation temperature $T_{elevation}$ due to the dissipated power is:

(equation 12.)

$$T_{elevation} = R_{th} \times P_{tot}$$

The junction temperature T_j is:

(equation 13.)

$$T_j = T_{elevation} + T_{ambient}$$

5.1.4 example - conditions of use

- $V_{CC\,max}$ = 5.5V
- $I_{CC\,max}$ = 120mA
- $V_{DSsat\,max}$ = 0.4V
- $I_{output\ ports\,max}$ = 20mA
- $R_{pull\text{-}up}$ = 15kΩ
- PCB827-3 ⇒ $R_{th\ j\text{-}a}$ = 96.5°C/W

⇒ $P_{tot\,max}$ = 686mW
⇒ $T_{elev\,max}$ = 66.2°C

T_j is limited to 150°C therefore the ambient temperature must not exceed:

$T_{ambient\,max}$ = 84°C.

6 PRINCIPLE OF THE LOW NOISE PLL

6.1 Low noise PLL standard architecture

The phase noise performances required for the digital reception are far more important than for analogue standards. For 10kHz and 100kHz frequency offsets, the phase noise requirements are usually achieved by the “free running” VCO phase noise characteristics, but the 1kHz offset target (in case of OFDM reception) cannot be reached by the conventional MOPLL architecture. The TDA6650/51TT uses the phase noise properties of the PLL to improve the global phase noise characteristic (see figure 67).

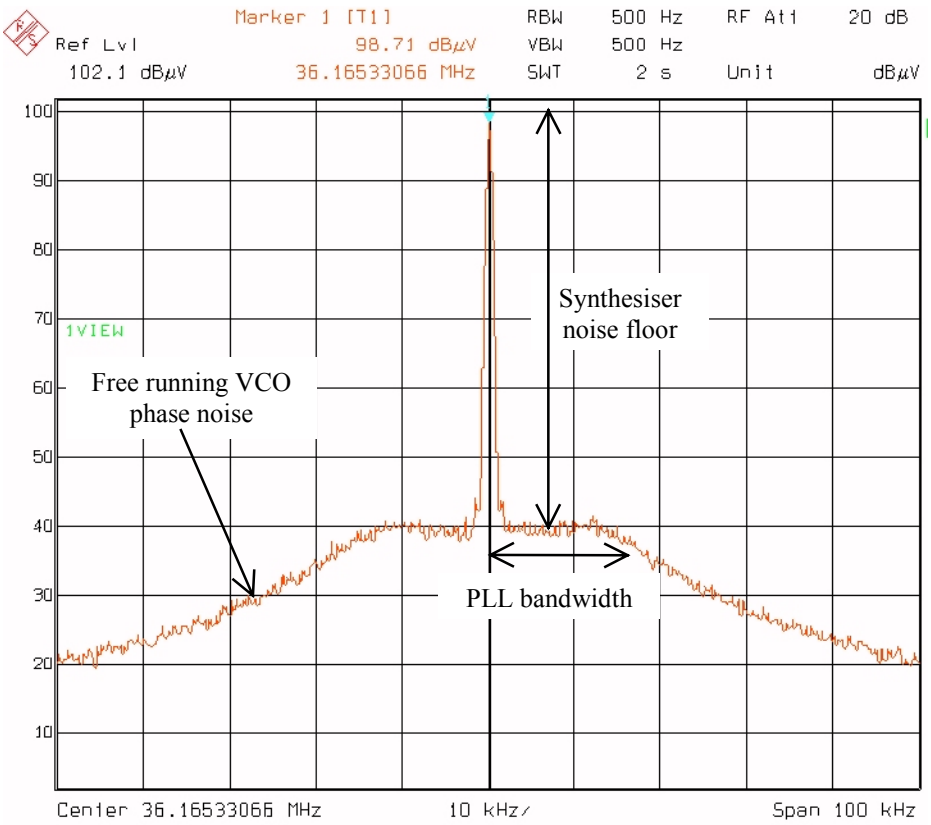


figure 67. Phase noise characteristics.

In the previous spectrum, the phase noise is “cleaned” within the operating area of the PLL (PLL bandwidth). In this area the phase noise is maintained to the “synthesizer noise floor”. This synthesizer noise floor is directly linked to the noise characteristics of the PLL reference chain and to the AC loop response. (The reference chain is made up with the Xtal oscillator, the reference divider and the phase detector - charge pump. The PLL bandwidth is determined by the loop filter application.)

The VCO phase noise in closed loop application can be split into two parts:
- The noise contribution coming from the PLL reference chain.
- The noise contribution coming from the VCO itself.

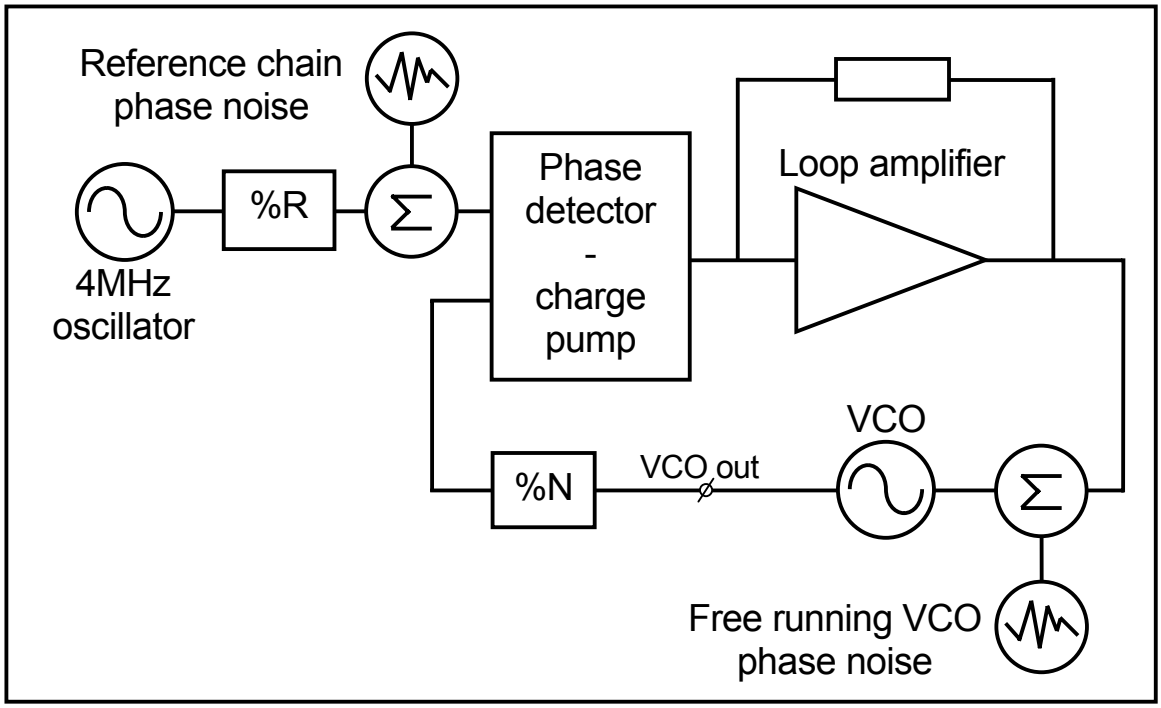


figure 68. Simplified noise model of the PLL-VCO loop.

The transfer functions from each of the noise source to the closed loop VCO output are:

(equation 14.)
$$H_{ref}(p) = N \times \frac{G(p)}{1+G(p)}$$

H_{ref} transfer from the reference chain noise to the VCO output

(equation 15.)
$$H_{vco}(p) = \frac{1}{1+G(p)}$$

H_{vco} transfer from the free running VCO phase noise to the VCO output

with $$G(p) = \frac{I_{cp} \times K_{vco}}{N \times p^2 \times C_1} \times \frac{(1+p \times R_1 \times C_1)}{(1+p \times R_1 \times C_2) \times (1+p \times R_p \times C_p)}$$

I_{cp} charge pump current
K_{vco} VCO slope
N main divider ratio
C_1, C_2, C_p, R_1, R_p components of the loop filter.

The two phase noise transfers are depicted below (typical examples).

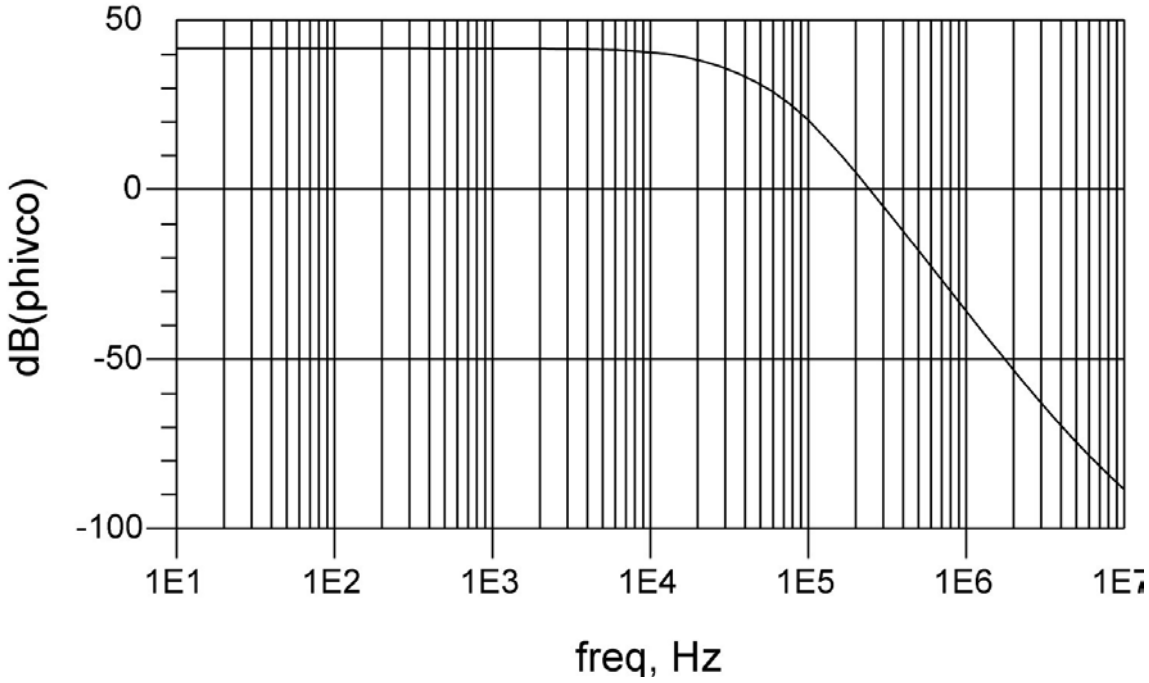


figure 69. Example of H_{ref} transfer.

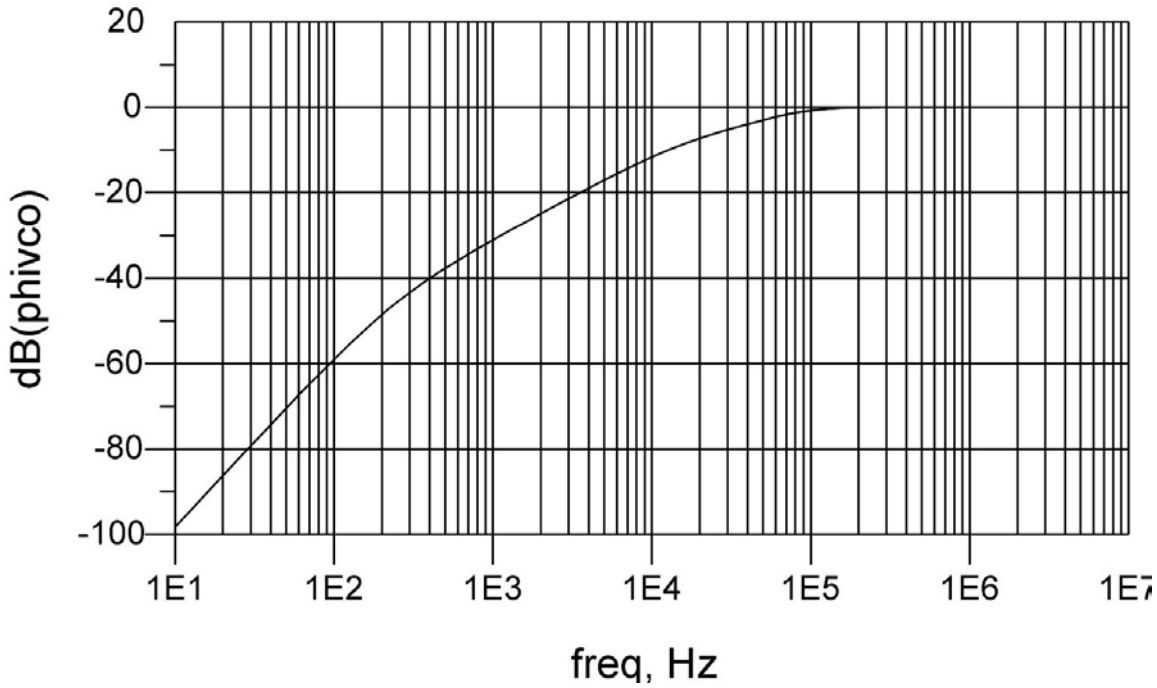


figure 70. Example of H_{vco} transfer.

↳ The noise contribution from the reference chain is transferred to the VCO output through a low pass function.

↳ The phase noise contribution of the free running VCO is transferred through a high pass function.

As a conclusion:
- for low frequency offsets (within the PLL bandwidth), the phase noise is mainly due to the reference chain whereas the free running VCO phase noise is rejected
- On the opposite for high frequency offsets, the phase noise contribution from the reference chain is filtered whereas the free running VCO phase noise is directly transferred.

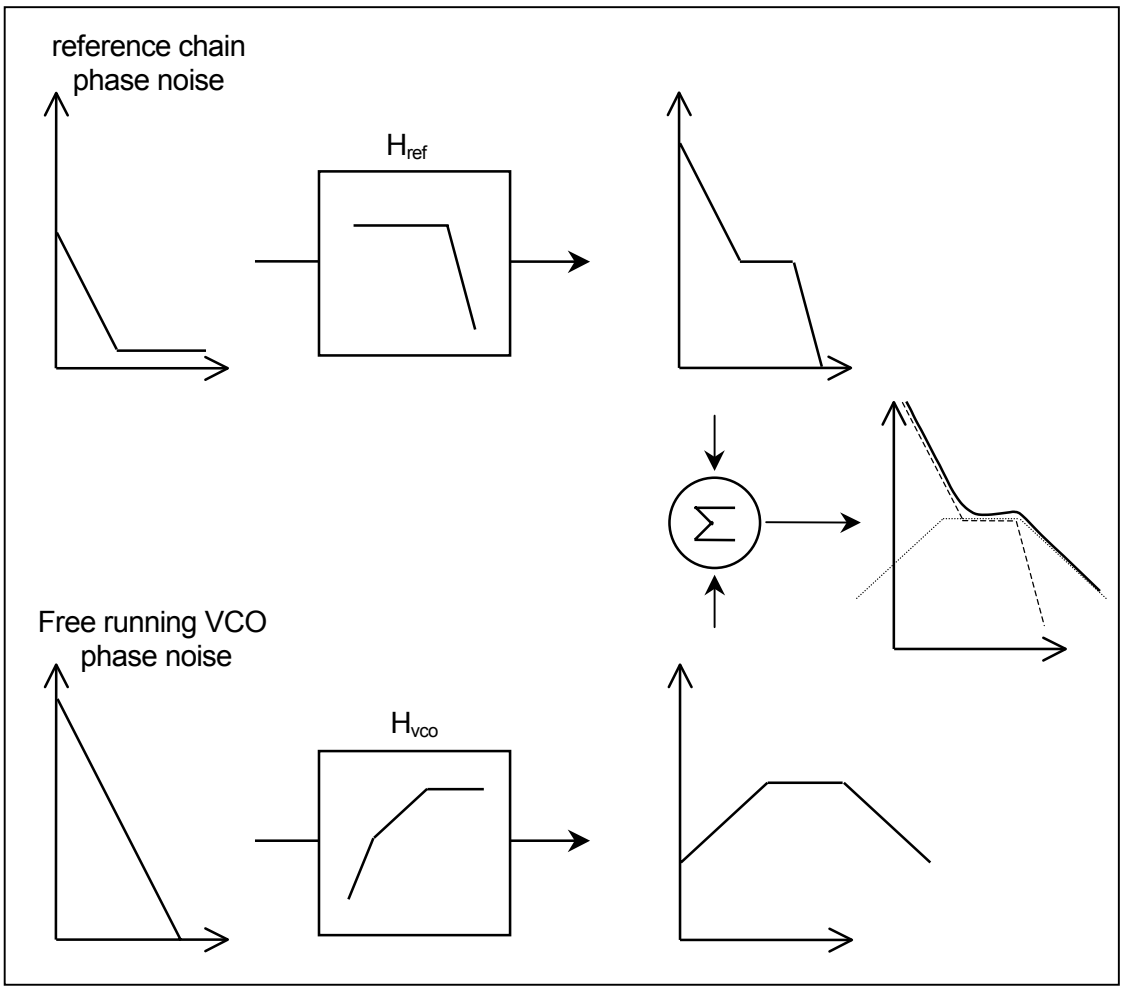


figure 71. Phase noise contributions.

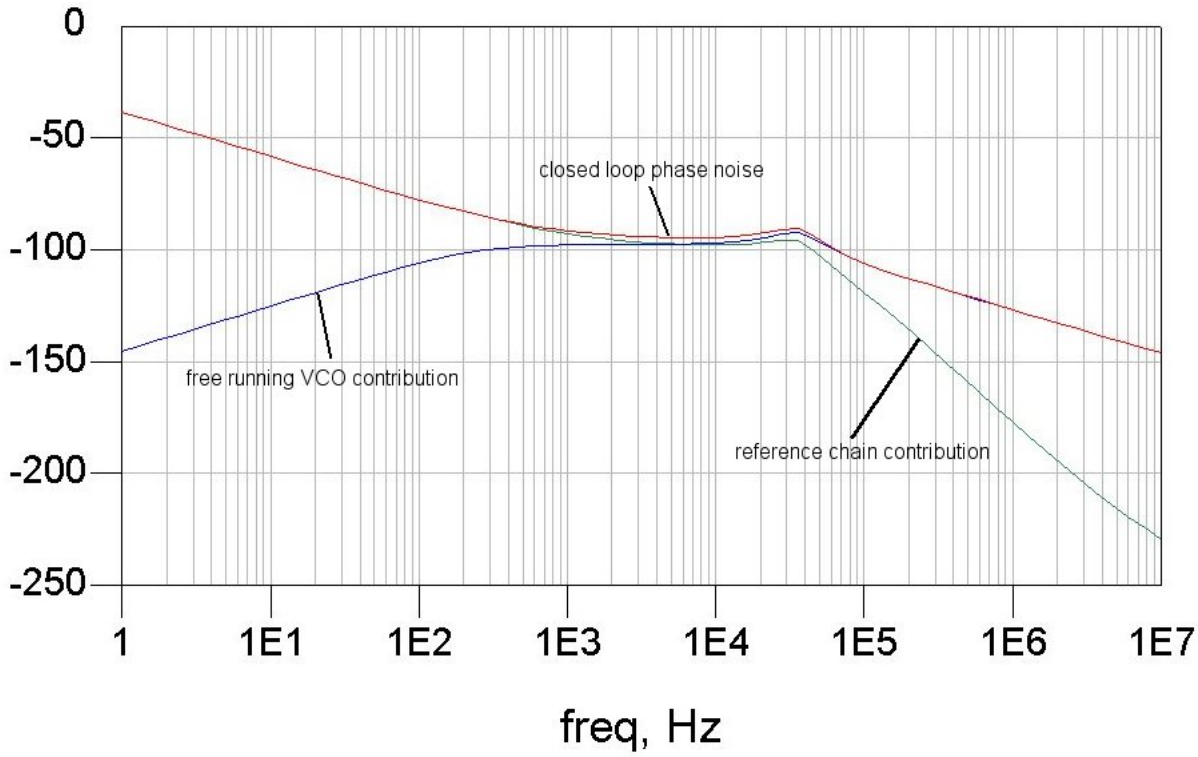


figure 72. Example of closed loop phase noise.

The VCO closed loop spectrum can be improved for low frequency offsets provided the reference chain noise contribution is low and provided the PLL bandwidth is wide enough.

The Low Noise PLL / MOPLL(such as TSA5060A, TSA5059, TDA6650/51) intend to cope with both of those two requirements.

6.2 Limitations in the standard architecture

The first way to improve the phase noise at low frequency offset is to reduce the reference chain contribution, which means design low noise Xtal oscillator, low noise reference divider and low noise phase detector charge-pump.

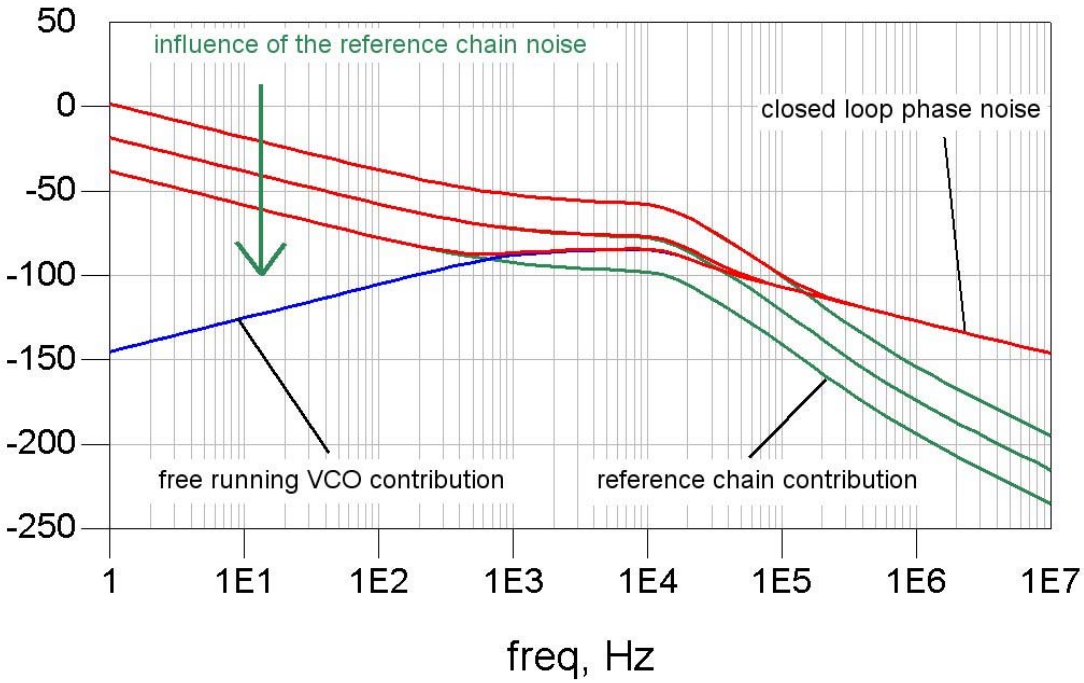


figure 73. Influence of the improvement of the reference chain noise.

- For low frequency offsets (in the previous example below 1kHz), the reference chain contribution always dominates.
- For high frequency offsets (higher than 200kHz), the free running VCO always dominates.
- For intermediate offsets, the closed loop phase noise copies the reference chain contribution, excepted if the free running VCO contribution is too high: in the previous example, in the lower curve, the improvement cannot be exploited (between 1kHz and 200kHz).

The only way to exploit the reference chain noise improvement is to lower the free running VCO contribution. This can be done either by improving the intrinsic free running VCO phase noise (see figure 74) or by increasing the PLL bandwidth (see figure 75 & figure 76).

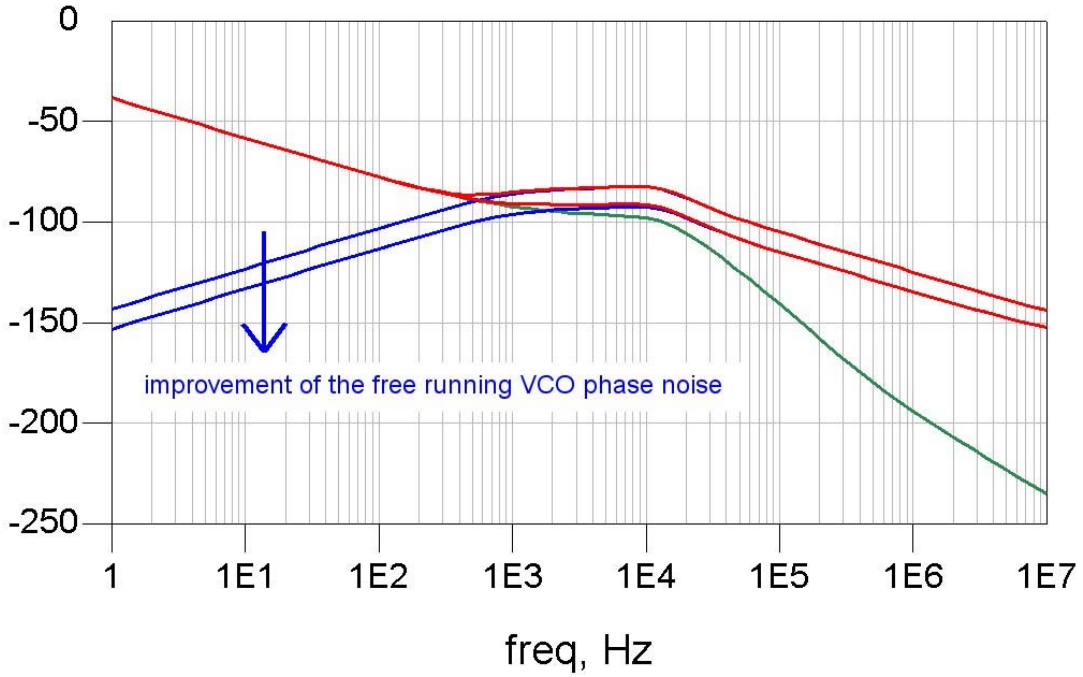


figure 74. Influence of the free running VCO phase noise improvement

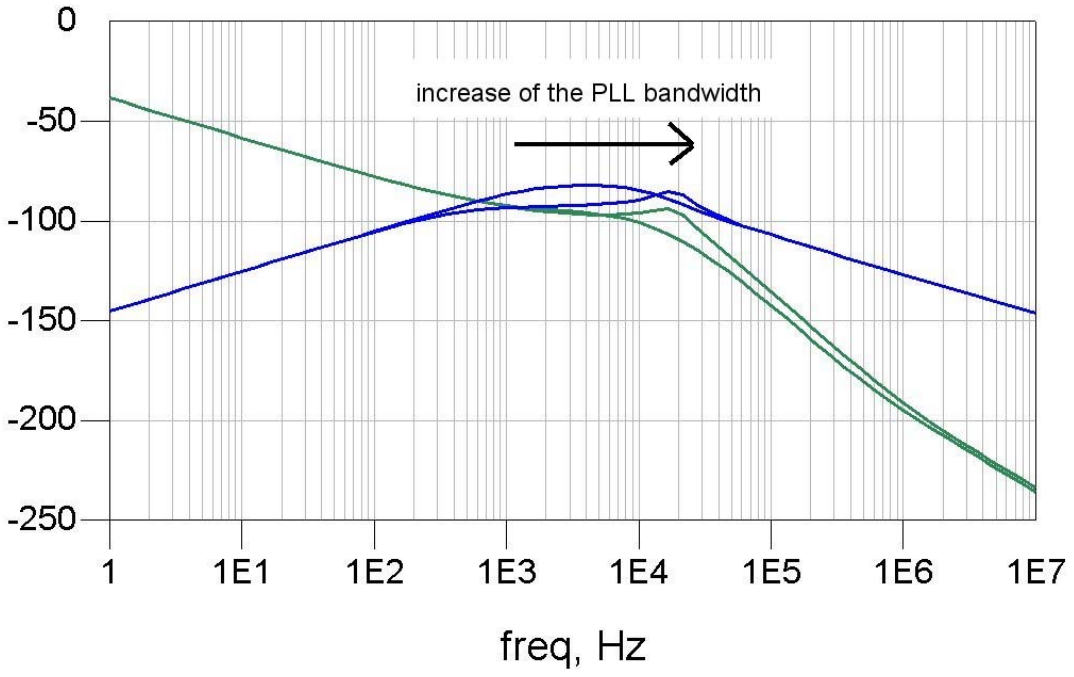


figure 75. Effect of the PLL bandwidth increase (contributions of the reference chain and of the free running VCO) (1)

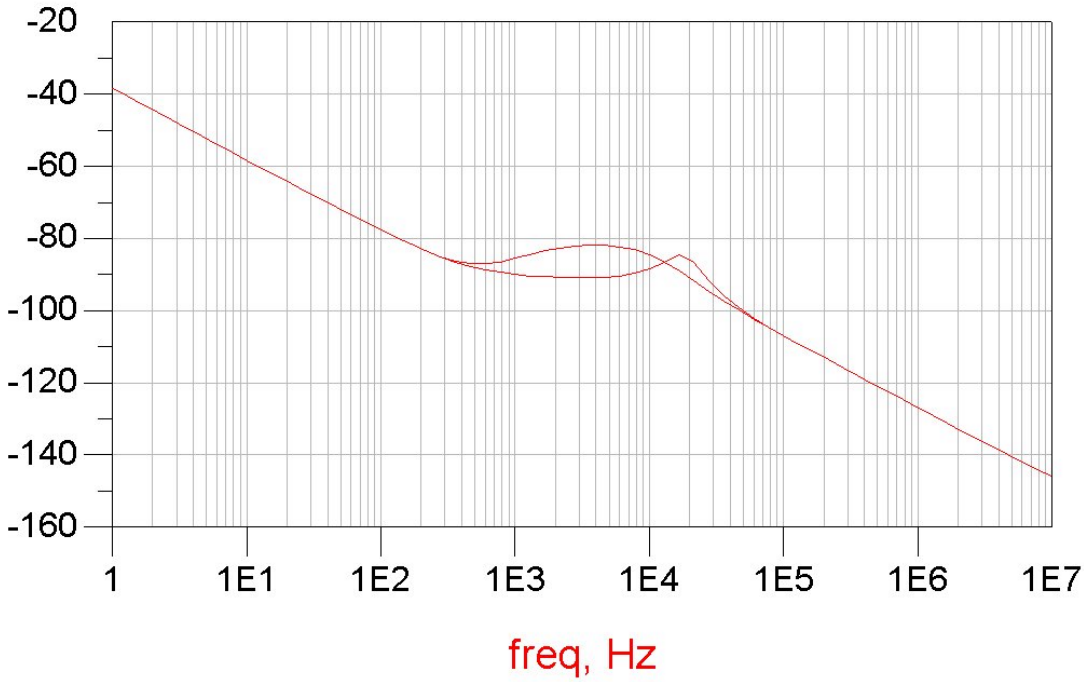


figure 76. Effect of the PLL bandwidth increase (closed loop phase noise) (2)

Limitations:
- The intrinsic free running VCO phase noise is more or less fixed.
- The PLL bandwidth is limited by stability requirements, in practice, it cannot really be higher than 1/10 of the synthesizer comparison frequency without stability troubles.

6.3 Fractional-N synthesizer

6.3.1 Phase noise considerations

In standard PLL architecture, the frequency step, f_{step}, is also the operating frequency of the phase detector (also called comparison frequency f_{comp}) . The frequency step is fixed by the standard, therefore the comparison frequency is also fixed, and consequently, the PLL bandwidth cannot exceed a lot $\left(f_{comp} / 10 \right)$ (for stability reasons).

In fractional-N concept the comparison frequency and the step frequency can be split up. The step frequency can be chosen to be compatible with the targeted TV standard, and the comparison frequency can be increase to allow wide PLL bandwidth.

Moreover, a second effect improves the closed loop phase noise:

For a standard architecture: $f_{vco} = N \times f_{comp} = N \times f_{step}$

For a fractional-N architecture: $f_{vco} = N' \times f_{comp} \quad with\ f_{comp} > f_{step}$

Therefore for the same VCO frequency f_{vco} the "main divider ratio" is lower for the fractional-N synthesizer (N'<N). The synthesizer noise floor is linked to the main divider ratio (see figure 77).

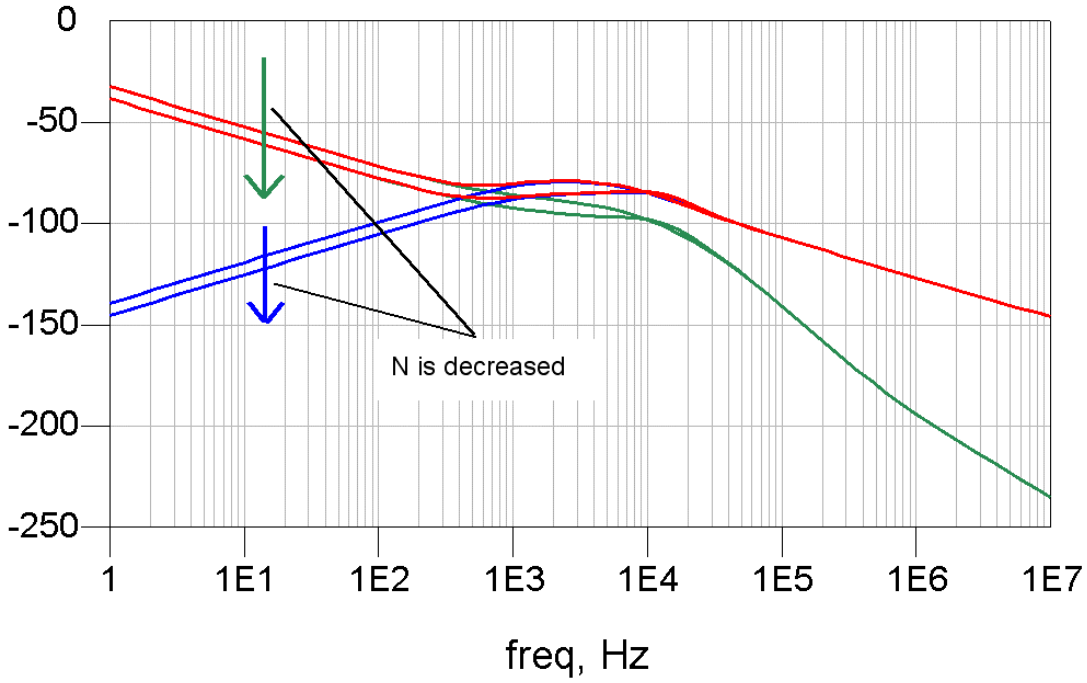


figure 77. Influence of the main divider ratio.

As a conclusion, the fractional-N architecture reaches good phase noise performances because:
1. it allows a high comparison frequency thus a large PLL bandwidth, and thus the reference chain noise reduction can be exploited.
2. It decreases the main divider ratio, and thus decreases the synthesizer noise floor.

6.3.2 Fractional-N principle

In the fractional-N architecture, the VCO frequency can be written as follow:

(equation 16.) $$f_{vco} = (I + \frac{k}{q}) \times f_{comp}$$ *with I, k and q integers.*

The step frequency is:

(equation 17.) $$f_{step} = \frac{1}{q} \times f_{comp}$$

The TDA6650/51TT uses the following correspondence:

f_{step}	f_{comp}	k	q	R0	R1	R2
62.5kHz	2MHz	$0 \le k \le 31$	32	0	0	0
142.86kHz	4MHz	$0 \le k \le 27$	28	1	0	0
166.67kHz	4MHz	$0 \le k \le 24$	24	0	1	0
50kHz	1MHz	$0 \le k \le 20$	20	1	1	0
125kHz	4MHz	$0 \le k \le 31$	32	0	0	1

Table 20. Fractional parameters in the TDA6650/51TT.

Example: f_{vco} = 240.25MHz & f_{step} = 62.5kHz

f_{step} = 62.5kHz $\Rightarrow f_{comp}$ = 2MHz, q = 32

(equation 18.)

$$I = Integer\ part\ of\ (\frac{f_{vco}}{f_{comp}})$$

&

(equation 19.)

$$k = \frac{q \times f_{vco}}{f_{comp}} - I \times q$$

$\Rightarrow I = 120 \quad \& \quad k = 4$

A conventional divider can divide only by an integer number and not a fractional number. The instantaneous ratio between the comparison period T_{comp} and the VCO period T_{vco} is always an integer. The fractional division is not an instantaneous division but the average result of several divisions.

During one comparison cycle (i.e. one comparison period) the main divider ratio is programmed to a fixed integer number N or (N+1). So the relation between T_{vco} and T_{comp} (instantaneous values) can be written as follows:

$$T_{comp} = N \times T'_{vco} \quad or \quad T_{comp} = (N+1) \times T''_{vco}$$

The divider ratio is switched between N and (N+1), according the following diagram:

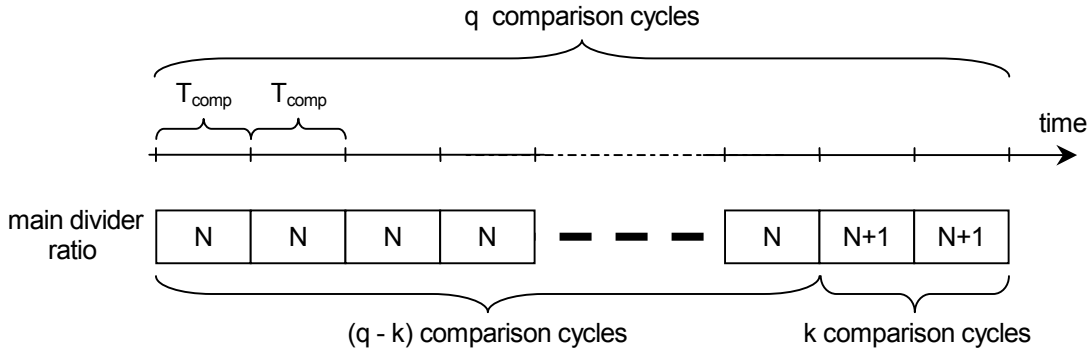


figure 78. Fractional-N division principle.

The average VCO period is obtained on q comparison periods.

$$
\begin{aligned}
q \times T_{comp} &= (q-k) \times T_{comp} + k \times T_{comp} \\
\Leftrightarrow q \times T_{comp} &= (q-k) \times N \times T_{vco} + k \times (N+1) \times T_{vco} \\
\Leftrightarrow q \times T_{comp} &= (q \times N + k) \times T_{vco}
\end{aligned}
$$

$$
\Leftrightarrow T_{comp} = (N + \frac{k}{q}) \times T_{vco}
$$

(equation 20.)

$$
\boxed{\Leftrightarrow f_{vco} = (N + \frac{k}{q}) \times f_{comp}}
$$

7 USING A DC-DC CONVERTER

In some tuners, the 30 Volts supply is delivered by an embedded DC-DC converter. Such an application must be designed carefully, it can impact the phase lock loop stability.

7.1 biasing of the loop

Before studying the PLL stability with a conventional AC model, it is mandatory to analyze (check) the biasing of the various building blocs in the loop.
That analysis is focused on the charge pump, the loop amplifier and on the DC-DC converter output.

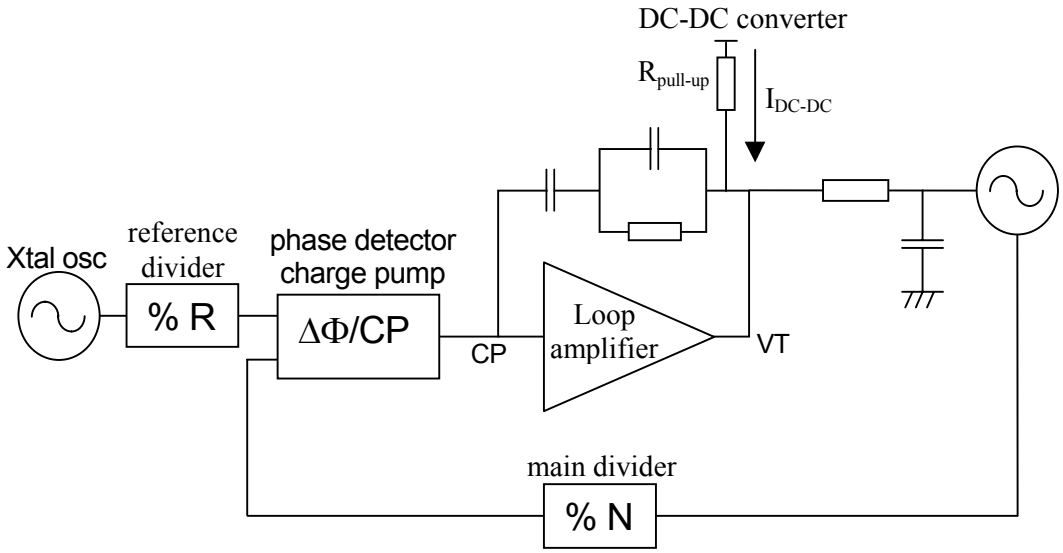


figure 79. Building blocs for the transient analysis.

For that analysis, it must be noted that:

⇨ The purpose of the PLL is to control the VT voltage that bias VCO tank circuit varicaps. Oscillator tank circuits are usually aligned so as to cover the required frequency range for VT voltages between 1V and 25V. (VCO alignment of the demonstration board).

⇨The current delivered to the PLL (to the charge pump, to the loop amplifier) can be simply calculated :

(equation 21.)

$$I_{DC-DC} = \left(\frac{V_{DC-DC\ converter} - VT}{R_{pull-up}} \right)$$

7.2 transient behavior

When a frequency jump is programmed from the low to the high end of a band, the loop filter has to be charged. The charge is performed thanks to the current delivered by the DC-DC converter.

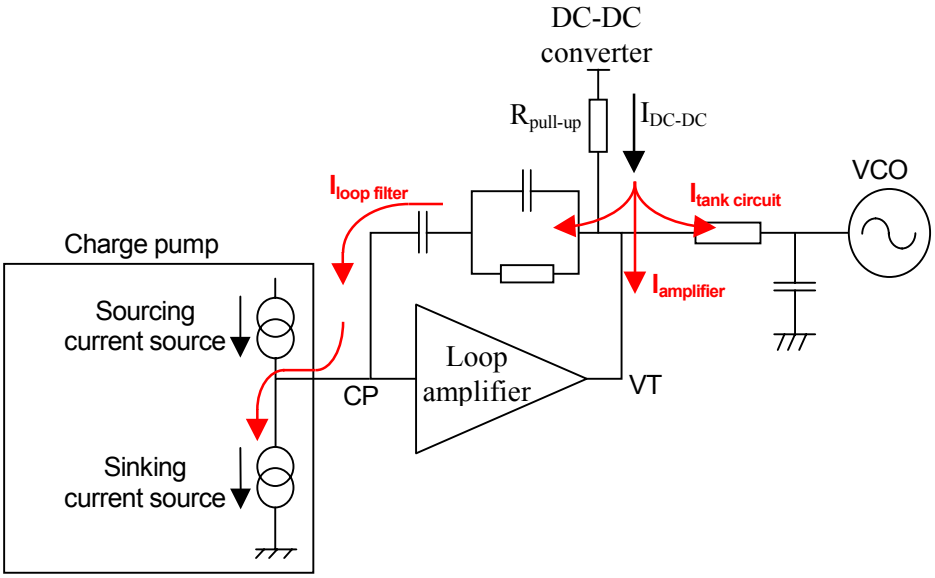


figure 80. Current distribution when loading the loop filter

The DC-DC converter supplies a current I_{DC-DC} which is then distributed to:

- The loop filter ($I_{loop\ filter}$)
- The loop amplifier output ($I_{amplifier}$)
- The VCO tank circuit ($I_{tank\ circuit}$)

The current loading the loop filter ($I_{loop\ filter}$) is absorbed by the charge pump sinking current source.

2 configurations may occur:

1. The DC-DC converter is able to drive a current higher than I_{CP}. (nominal condition)
2. The DC-DC converter capability is lower than I_{CP}.

7.3 Nominal biasing ($I_{DC-DC}>I_{CP}$)

7.3.1 Charge pump biasing

For a frequency jump from the low to the high end of a band, the charge pump can be model as a NPN current mirror. The sourcing current source is deactivated.
The charge pump acts as a current mirror, therefore the sinking current is determined by the choice of I_{CP}.

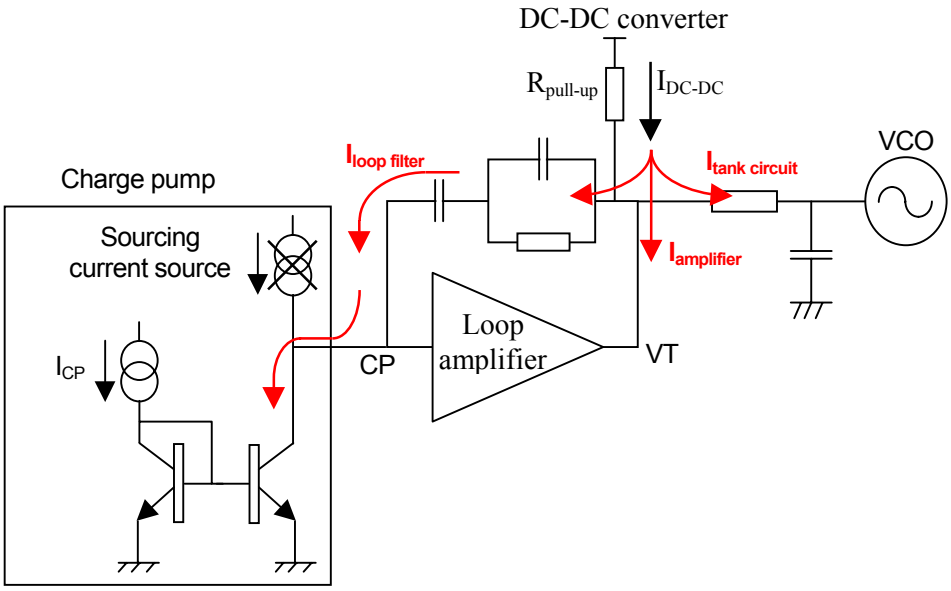


figure 81. Charge pump transient model.

This sinking current also loads the loop filter:

(equation 22.) $I_{loop\ filter} = I_{CP}$

7.3.2 Loop amplifier biasing

The loop amplifier behaves as a transconductance: the amplifier output current ($I_{amplifier}$) is determined by the amplifier input voltage (voltage at CP pin, V_{CP}). A simplified transfer characteristic is depicted below:

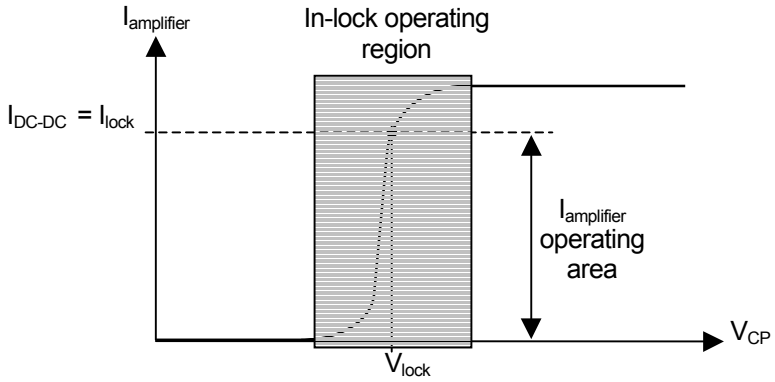


figure 82. Loop amplifier transfer characteristic.

Normal operation corresponds to:

(equation 23.) $I_{amplifier} \neq 0$

NB: $I_{amplifier}$ is limited by the maximum current available I_{DC-DC}.

7.3.3 In-lock status

In the “In-lock operating region” the loop amplifier has a high gain (high slope) (see figure 82). The conventional AC model used for stability analysis is valid in this area.
When the loop is finally locked, the loop filter as well as the VCO tank circuit are charged :

(equation 24.) $I_{loop\ filter} = 0 \ \ \& \ \ I_{tank\ circuit} = 0 \Rightarrow I_{amplifier} = I_{DC-DC}$

7.4 Critical condition ($I_{DC-DC} < I_{CP}$)

If the DC-DC converter has limited drive capabilities ($I_{DC-DC} < I_{CP}$), the transient behavior is impacted. Indeed the flowing current (see figure 81) is no longer limited by the charge pump but by the DC-DC converter. The current mirror enters in saturation mode, and as a consequence, the voltage at the output of the current mirror falls down to a Vce,sat.

During that saturation, the loop amplifier is biased at a point where there is no gain, the PLL conventional AC model is not valid under those conditions.

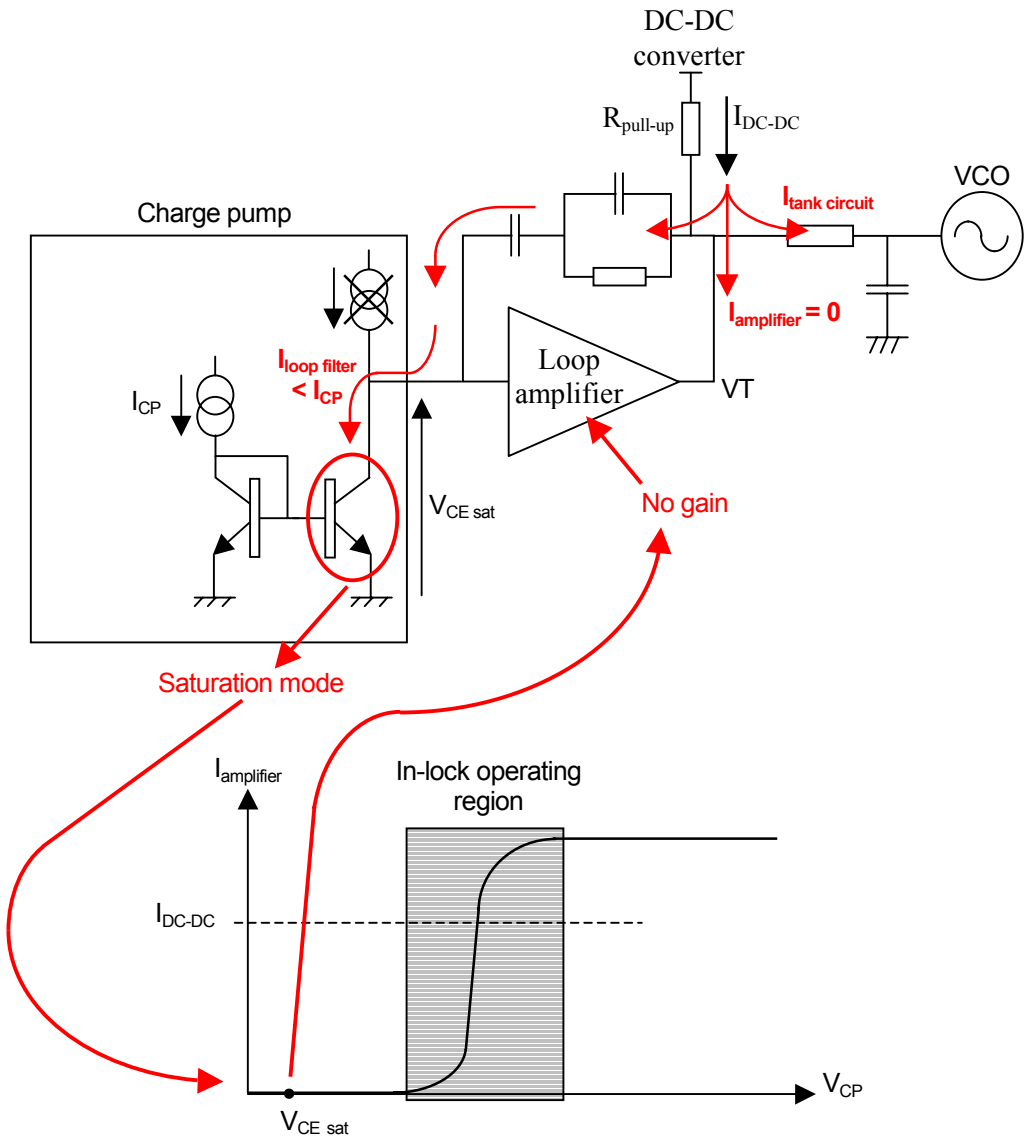


figure 83. biasing of the loop when $I_{DC-DC}<I_{CP}$.

7.5 practical configuration (demonstration board).

The limitation presented above also occurs when the supply voltage is limited.
For example, in case of the demonstration board, the supply voltage is 30V, the pull-up resistor is 15kΩ, in this case the current delivered is already below the highest CP current (600µA).

The maximum current which can be delivered by the source at the high end of the band (V_T=25V) is:

(equation 25.)

$$I_{max} = \left(\frac{30V - 25V}{15k\Omega} \right) = 333\mu A < 600\mu A$$

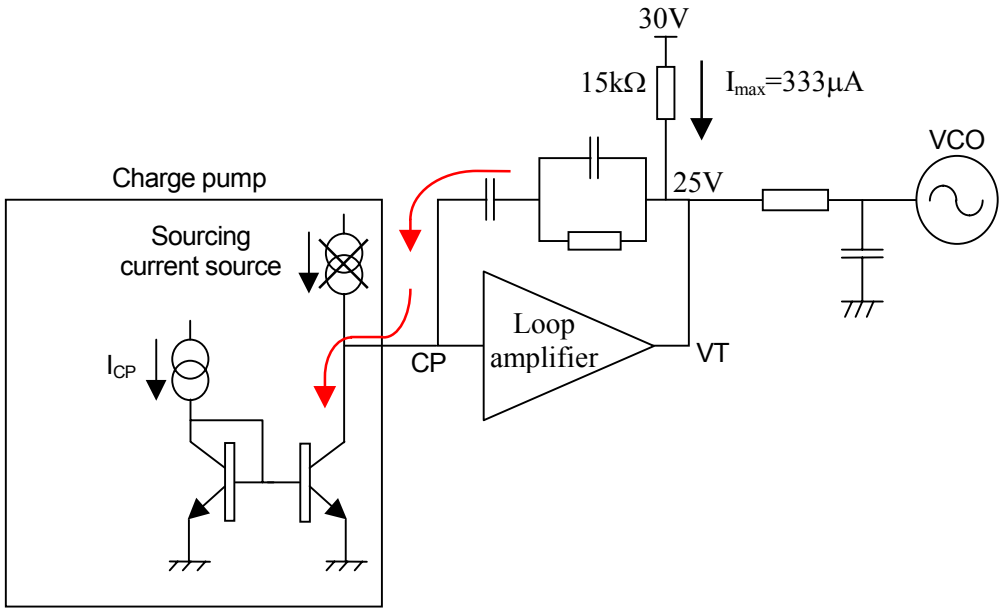


figure 84. Demonstration board configuration.

In that configuration, the loop is able to lock.

The power delivered by the supply source is:

(equation 26.) $P = 30V \times 333\mu A = 10mW$

In practice, when the loop is near the in-lock status, the charge pump structure is no longer permanently switched in the sinking configuration (see figure 85) therefore the current requirements to be delivered by the source are reduced in this area.
In that case the CP current is no longer a DC current, it becomes a dynamic or an average current. When the loop is locked, the loop filter is completely charged, there is no need for any current in the charge pump.

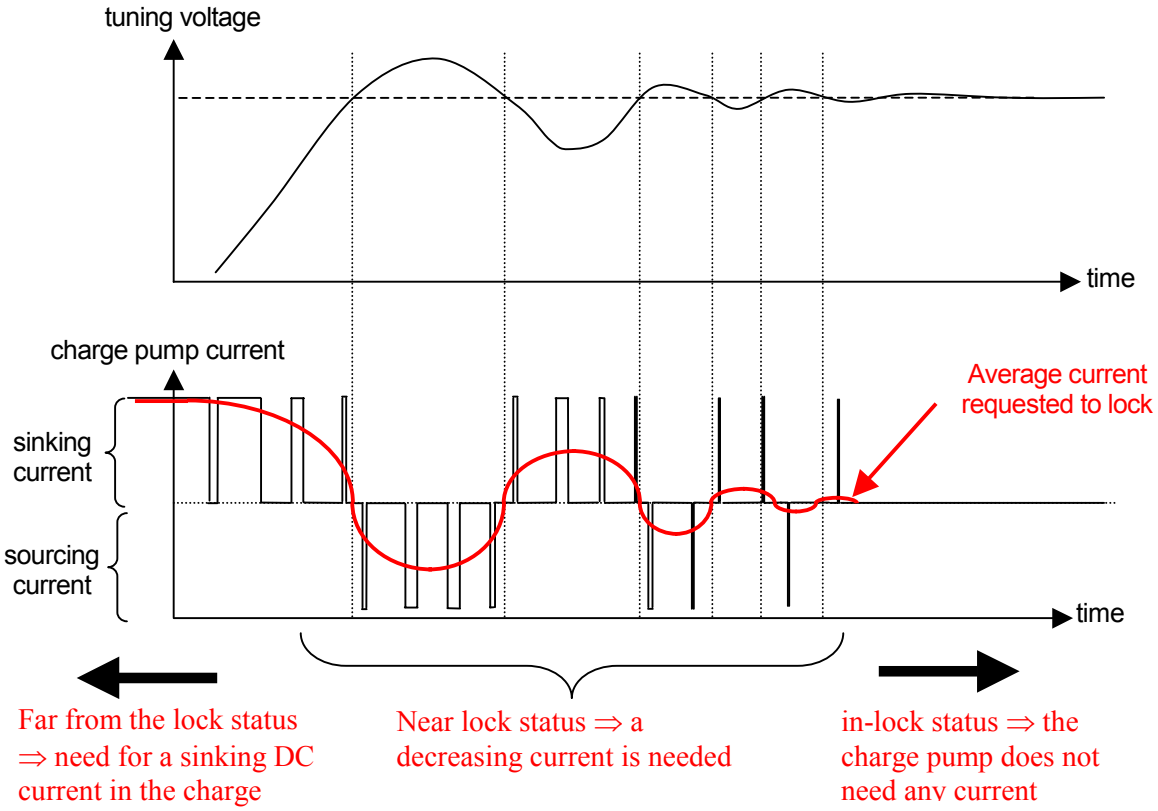


figure 85. current requirements during the locking time.

As the average required CP current is progressively decreasing, the saturation is less tremendous, and the CP output voltage increases (V_{CE} sat see figure 86).

⇨ If this voltage is able to reach the "in-lock operating region", the PLL will react according to the conventional AC model and will lock.

⇨ If this voltage is not able to reach this region (the saturation is too high), the PLL will not lock (unstable behavior).

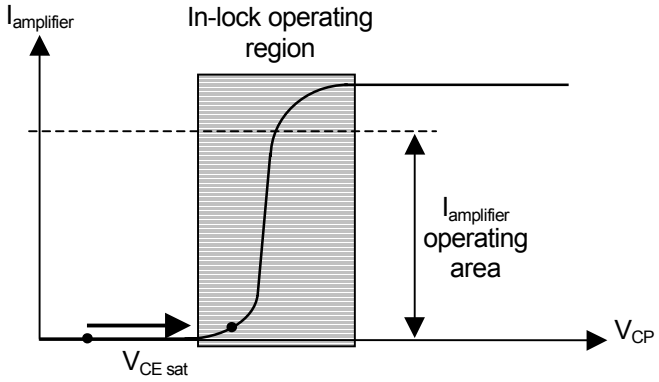


figure 86. Decreasing saturation

As a conclusion, the PLL can lock even if the DC-DC converter (or the supply source) delivers a current lower than I_{CP}. But this configuration must be avoided.

If it cannot be avoided, it is recommended to design an application which is able to deliver a current in line with the demonstration board configuration:

(equation 27.) $P_{DC\text{-}DC} \geq 10mW$

This configuration has been used for the IC qualification.

8 DEMONSTRATION BOARDS

The boards are designed to demonstrate the various features of the TDA6650/51TT.

The TDA6650TT is associated to the demonstration board PCB827-4.
The TDA6651TT is associated to the demonstration board PCB827-3.

This chapter only presents the PCB827-3 (TDA6651), but the second demonstration board (PCB827-4) is identical (mirrored version).

Some of those features need a customization of the demonstration board:
- I^2C bus protocol compatible with 2.5V, 3.3V and 5V micro-controllers (see paragraph 8.1.4 Jumpers / test point).
- 5 steps Analog to Digital converter (see paragraph 8.1.4 Jumpers / test point).
- Switched concept IF amplifier with both asymmetrical and symmetrical outputs.

The demonstration board configurations are described in the following paragraphs.

8.1 DEMONSTRATION BOARD DESCRIPTION

8.1.1 DC and I²C bus inputs:

J8 PLL control connector:

SCL	:	serial clock signal.
GND	:	ground.
SDA	:	serial data signal.
5V bus	:	5V bus (connected to the 5V bus of the J5 connector).
AS	:	address selection.

J5 Supply connector:

5V bus	:	5V bus (connected to the 5V bus of the J10 connector).
5V	:	TDA6650/51TT power supply.
30V	:	PLL tuning input voltage.
GND	:	ground.

8.1.2 RF inputs and IF output

J1, J2 High1, High2	:	High band differential RF signal input.
J3 MID	:	Mid band RF signal input.
J4 LOW	:	Low band RF differential signal input.
J6 IF out	:	IF signal output (the differential IF output of the IC is connected to a 10:2 transformer (TR1).

NB: The loss through this transformer is around 15.4 dB.

8.1.3 4MHz / Test output

J7 XT out	:	Crystal frequency buffer output, this connector is also used to output tests signals ½ fdiv and fcomp).

8.1.4 Jumpers / test point

ST1 BVS : I^2C Bus voltage selection.

Middle point of the jumper ST1	Bus voltage	Logic 0 levels	Logic 1 levels
Shorted to ground	2.5V	0V – 0.75V	1.75V – 5.5V
Open	3.3V	0V – 1.0V	2.3V – 5.5V
Shorted to 5V	5V	0V – 1.5V	3.0V – 5.5V

Table 21. I^2C Bus voltage selection.

ST2 ADC : PMOS open drain output port BS5 or ADC input.

Voltage applied on the middle point of ST2	A2	A1	A0
0.6 V_{CC} to V_{CC}	1	0	0
0.45 V_{CC} to 0.6 V_{CC}	0	1	1
0.3 V_{CC} to 0.45 V_{CC}	0	1	0
0.15 V_{CC} to 0.3 V_{CC}	0	0	1
0 to 0.15 V_{CC}	0	0	0

Table 2: A/D converter levels.

TP1 AGC : AGC detector output voltage.

8.2 Schematic diagram - symmetrical IF output

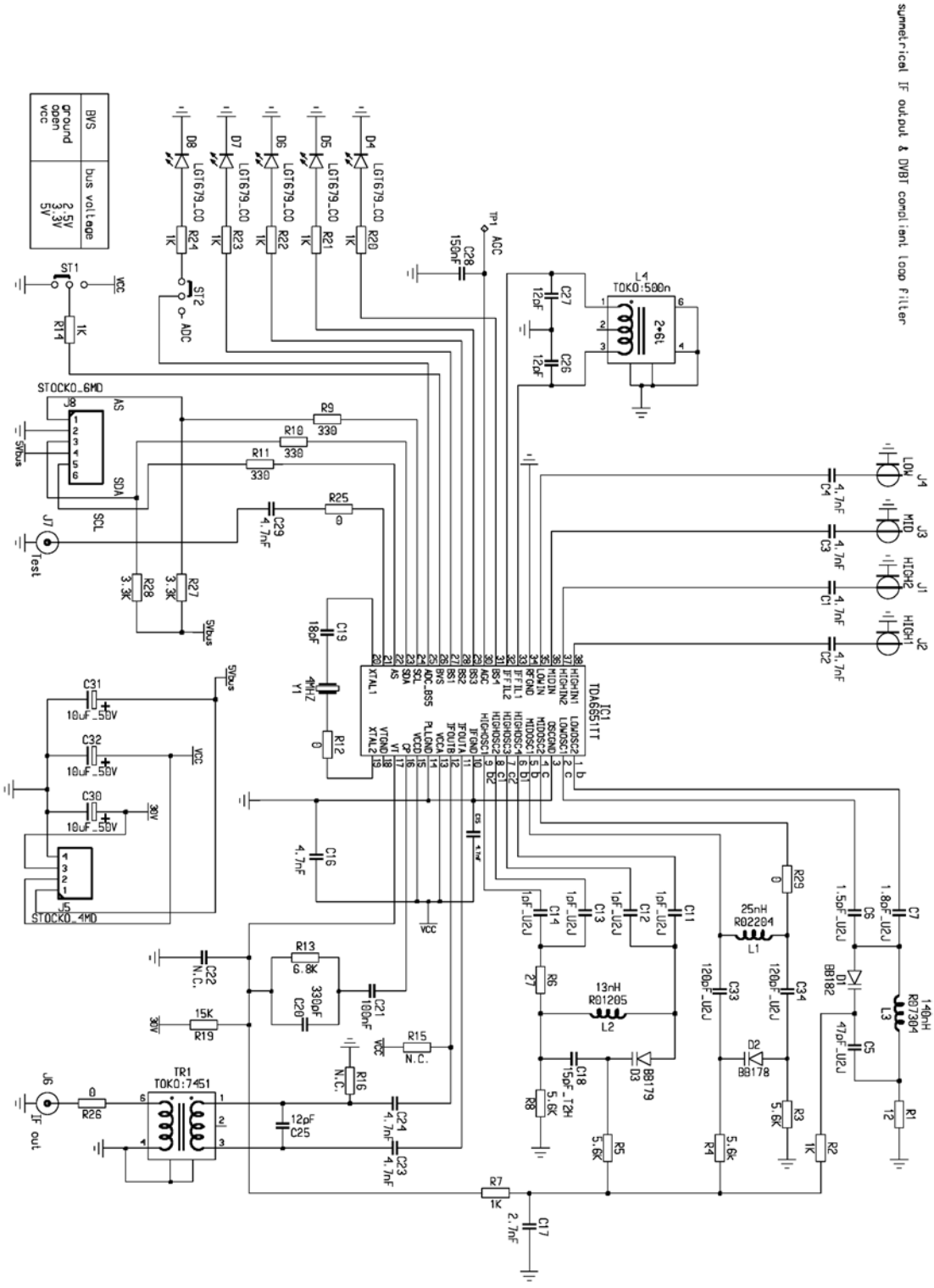


figure 87. schematic diagram with symmetrical IF output (PCB827-3)

8.3 Layouts

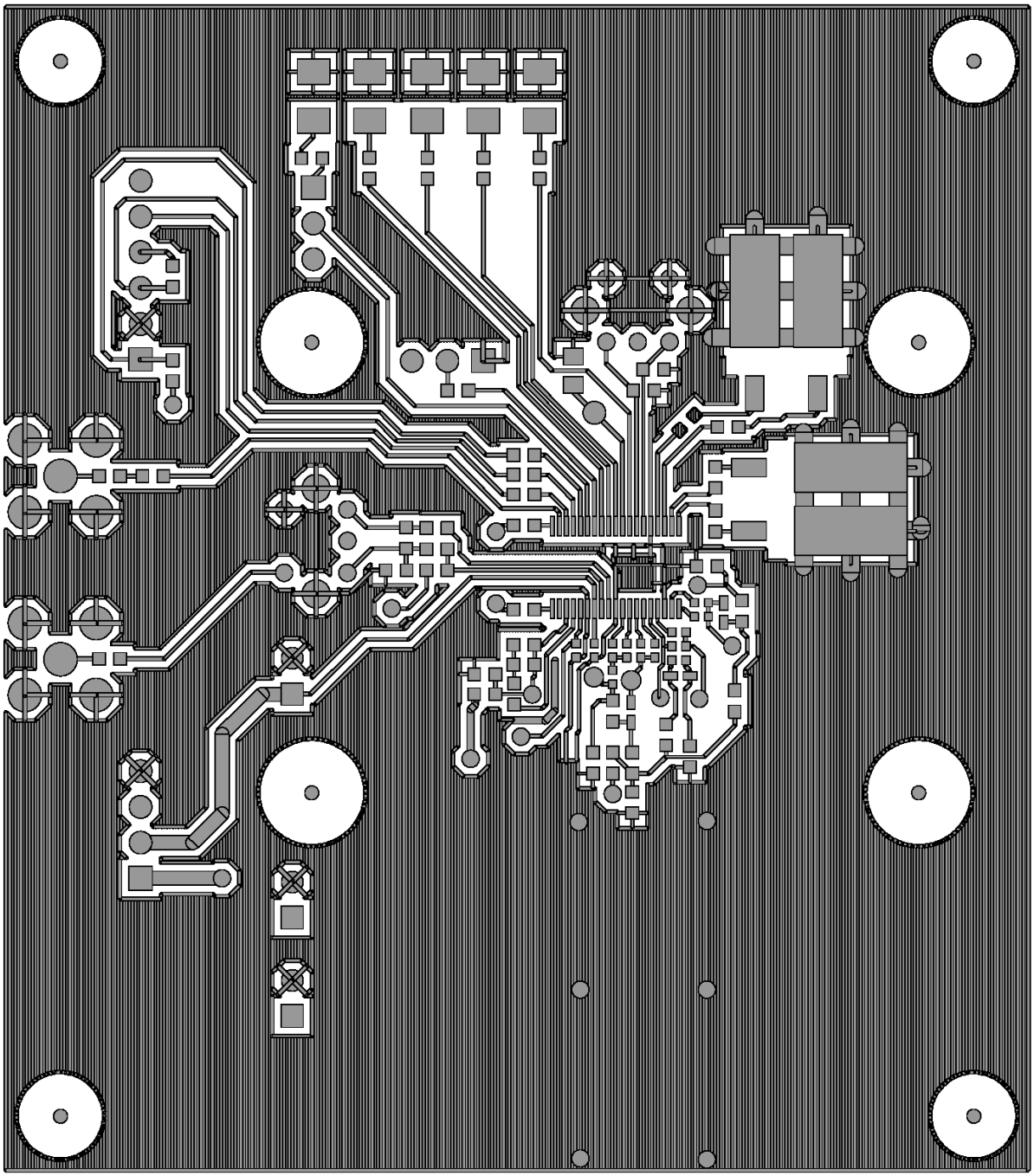


figure 88. PCB layout, top view.

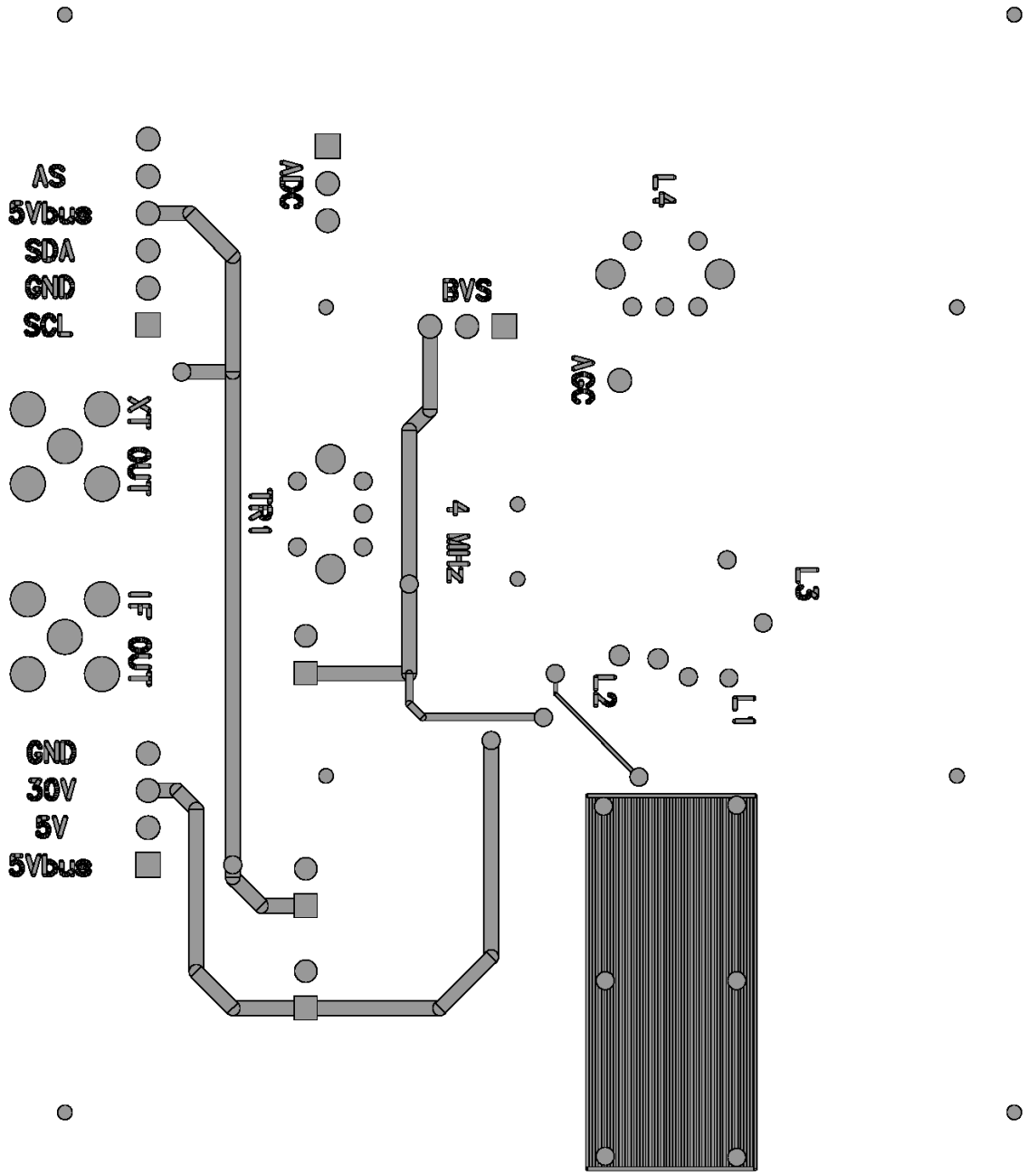


figure 89. PCB layout, rear view

8.4 Components placement

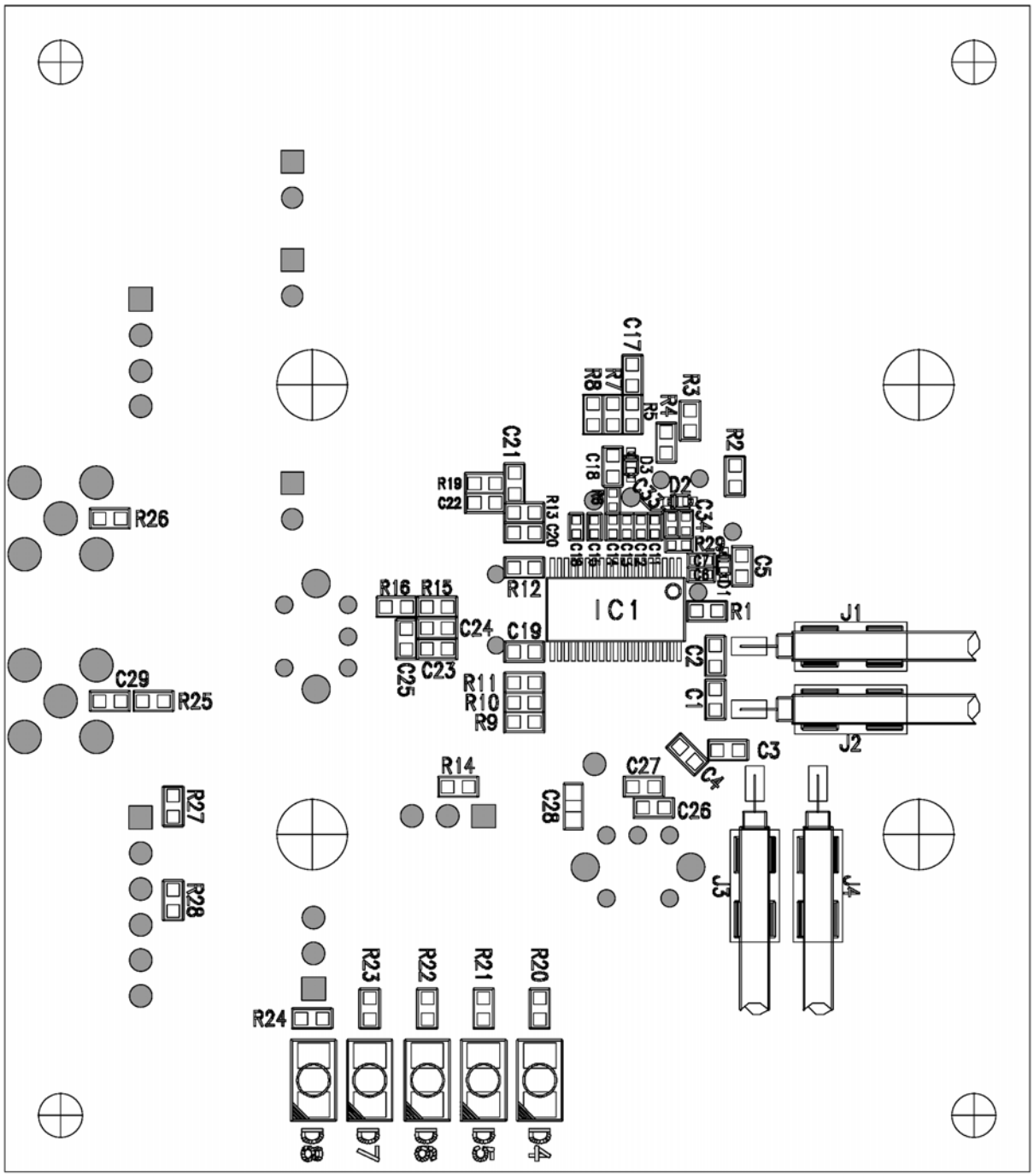


figure 90. Components placement, top view.

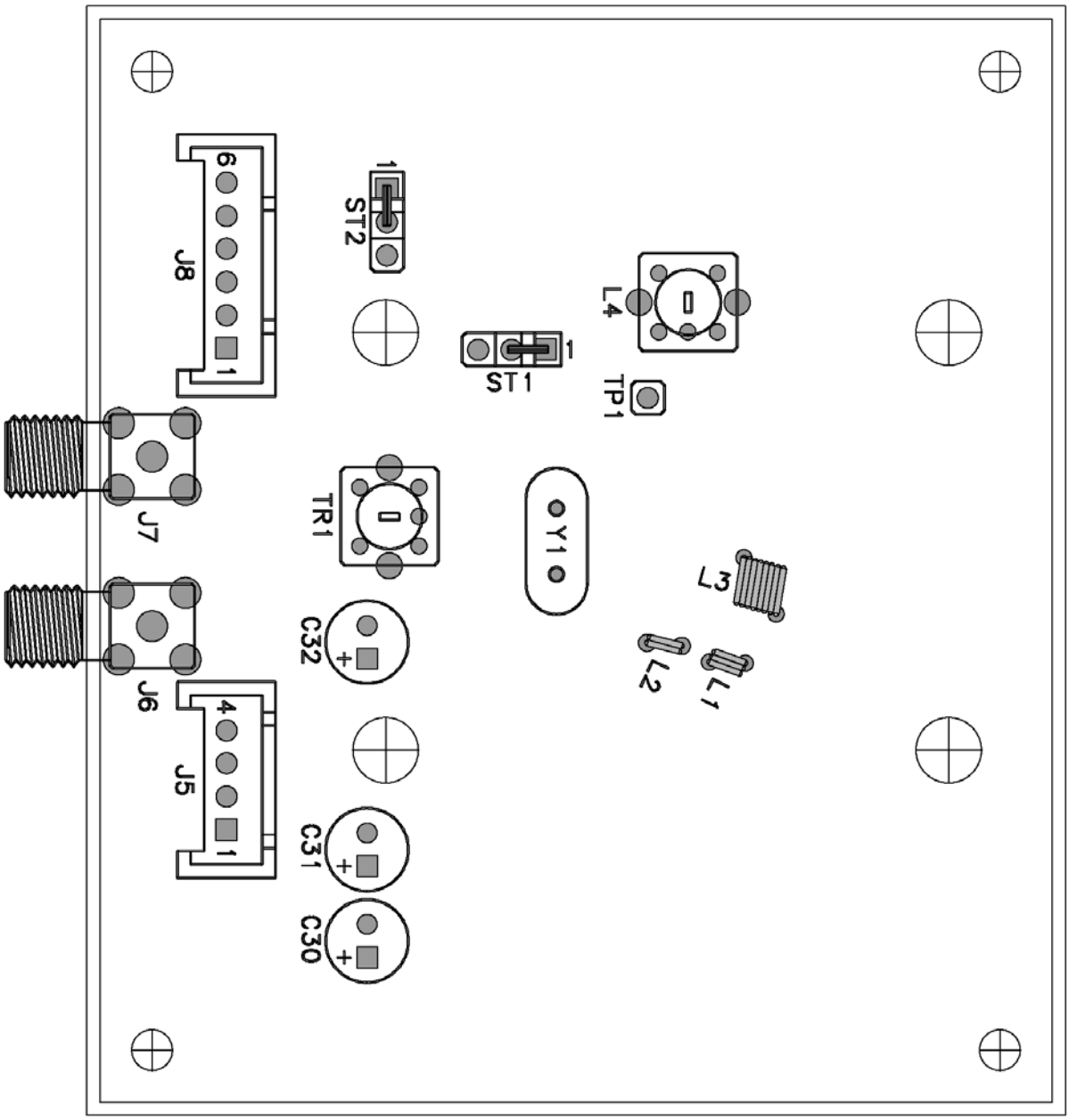


figure 91. Components placement, rear view.

8.5 Components list

REFERENCE	GEOMETRY	VALUE	SPECIFICATION
C1	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C2	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C3	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C4	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C5	c0603	47pF_U2J	Capacitor,CER2,0603,U2J,50V,-750+-120ppm
C6	c0402	1.5pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C7	c0402	1.8pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C11	c0402	1pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C12	c0402	1pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C13	c0402	1pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C14	c0402	1pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C15	c0402	4.7nF	Capacitor,CER2,0402,X7R,16V,10%
C16	c0402	4.7nF	Capacitor,CER2,0402,X7R,16V,10%
C17	c0603	2.7nF	Capacitor,CER2,0603,X7R,50V,10%
C18	c0603	15pF_T2H	Capacitor,CER2,0603,T2H,50V,-470+-60ppm
C19	c0603	18pF	Capacitor,CER2,0603,GOG,50V,5%
C20	c0603	330pF	Capacitor,CER2,0603,GOG,50V,5%
C21	c0603	100nF	Capacitor,CER2,0603,X7R,25V,10%
C22	c0603	N.C.	Capacitor,CER2,0603,***NO,CONNECTED***
C23	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C24	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C25	c0603	12pF	Capacitor,CER2,0603,GOG,50V,5%
C26	c0603	12pF	Capacitor,CER2,0603,GOG,50V,5%
C27	c0603	12pF	Capacitor,CER2,0603,GOG,50V,5%
C28	c0805	150nF	Capacitor,CER2,0805,X7R,25V,10%
C29	c0603	4.7nF	Capacitor,CER2,0603,X7R,50V,10%
C30	crt_d5	10uF_50V	PHILIPS:RSM037,Electrolytic,Capacitor,20%
C31	crt_d5	10uF_50V	PHILIPS:RSM037,Electrolytic,Capacitor,20%
C32	crt_d5	10uF_50V	PHILIPS:RSM037,Electrolytic,Capacitor,20%
C33	c0402	120pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
C34	c0402	120pF_U2J	Capacitor,CER2,0402,U2J,50V,-750+-120ppm
D1	sod523	BB182	PHILIPS:VHF,Variable,Capacitance,Diode,SMD,30V
D2	sod523	BB178	PHILIPS:VHF,Variable,Capacitance,Diode,SMD,30V
D3	sod523	BB179	PHILIPS:UHF,Variable,Capacitance,Diode,SMD,30V
D4	topled	LGT679_CO	SIEMENS:Diode,Topled,Green,2mA
D5	topled	LGT679_CO	SIEMENS:Diode,Topled,Green,2mA
D6	topled	LGT679_CO	SIEMENS:Diode,Topled,Green,2mA
D7	topled	LGT679_CO	SIEMENS:Diode,Topled,Green,2mA
D8	topled	LGT679_CO	SIEMENS:Diode,Topled,Green,2mA
IC1	sot510_1	TDA6651TT	PHILIPS:5V,Mixer,Oscillator,and,Low,Noise
J1	emp_rg405	EMP_RG405	coax
J2	emp_rg405	EMP_RG405	coax

REFERENCE	GEOMETRY	VALUE	SPECIFICATION
J3	emp_rg405	EMP_RG405	coax
J4	emp_rg405	EMP_RG405	coax
J5	stocko_4md	STOCKO_4MD	Connector,Straight,Male,1x4pins,2.54mm
J6	sma_fc	SMA_DIGIT	SMA,Connector,Right-Angle,Female
J7	sma_fc	SMA_DIGIT	SMA,Connector,Right-Angle,Female
J8	stocko_6md	STOCKO_6MD	Connector,Straight,Male,1x6pins,2.54mm
L1	self_r02204	R02204	self
L2	self_r01205	R01205	self
L3	self_r07304	R07304	self
L4	toko7km	TOKO:500n	trf_5c
R1	r0603	12	Resistor,Package:0603,5%,1/16W
R2	r0603	1K	Resistor,Package:0603,5%,1/16W
R3	r0603	5.6K	Resistor,Package:0603,5%,1/16W
R4	r0603	5.6k	Resistor,Package:0603,5%,1/16W
R5	r0603	5.6K	Resistor,Package:0603,5%,1/16W
R6	r0402	27	Resistor,Package:0402,5%,1/16W
R7	r0603	1K	Resistor,Package:0603,5%,1/16W
R8	r0603	5.6K	Resistor,Package:0603,5%,1/16W
R9	r0603	330	Resistor,Package:0603,5%,1/16W
R10	r0603	330	Resistor,Package:0603,5%,1/16W
R11	r0603	330	Resistor,Package:0603,5%,1/16W
R12	r0603	0	Resistor,Package:0603,5%,1/16W
R13	r0603	6.8K	Resistor,Package:0603,5%,1/16W
R14	r0603	1K	Resistor,Package:0603,5%,1/16W
R15	r0603	N.C.	Resistor,Package:0603,***NO,CONNECTED***
R16	r0603	N.C.	Resistor,Package:0603,***NO,CONNECTED***
R19	r0603	15K	Resistor,Package:0603,5%,1/16W
R20	r0603	1K	Resistor,Package:0603,5%,1/16W
R21	r0603	1K	Resistor,Package:0603,5%,1/16W
R22	r0603	1K	Resistor,Package:0603,5%,1/16W
R23	r0603	1K	Resistor,Package:0603,5%,1/16W
R24	r0603	1K	Resistor,Package:0603,5%,1/16W
R25	r0603	0	Resistor,Package:0603,5%,1/16W
R26	r0603	0	Resistor,Package:0603,5%,1/16W
R27	r0603	3.3K	Resistor,Package:0603,5%,1/16W
R28	r0603	3.3K	Resistor,Package:0603,5%,1/16W
R29	r0402	0	Resistor,Package:0402,5%,1/16W
ST1	cav_2p	CAV_2POS	Header,Single,Row,Straight,Pitch:2.54
ST2	cav_2p	CAV_2POS	Header,Single,Row,Straight,Pitch:2.54
TP1	tp0.9	TEST_Bar1	Header,Single,Row,Straight,1,pin
TR1	toko7km	TOKO:7451	trf_5b
Y1	hc49s	4MHZ	KONY:Quartz,Crystal,LowProfile,Package:HC49S

8.6 Schematic diagram - asymmetrical IF output

The IF amplifier can be switched in asymmetrical mode so as to drive a low impedance (75Ω). When the TDA6650/51TT is used in this asymmetrical mode, the IFOUTB pin needs to be connected to the supply voltage V_{CC}. The schematic of the new application is described in figure 92.

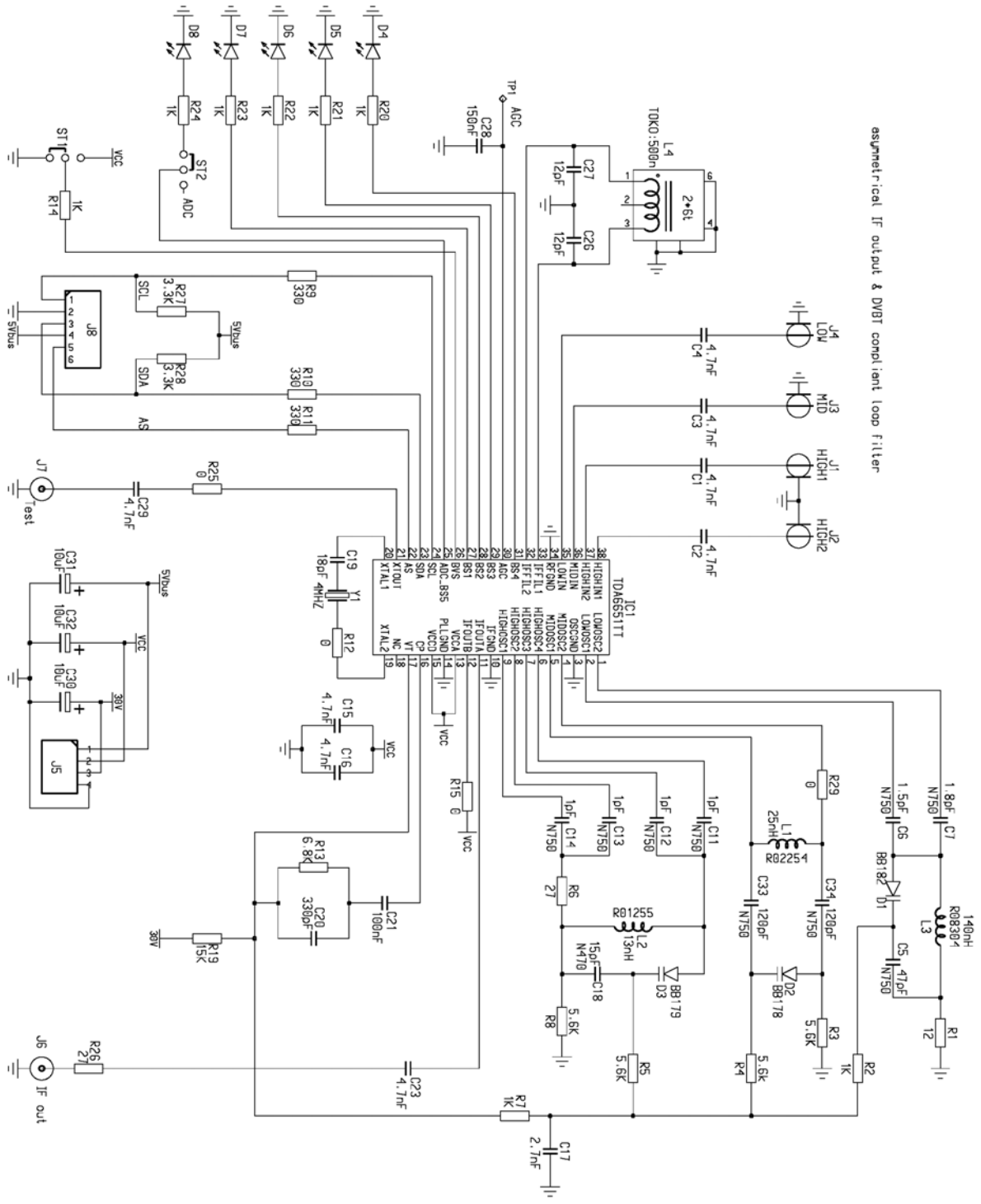


figure 92. schematic diagram with asymmetrical IF output

8.7 Board modifications in asymmetrical mode

The demonstration board has to be modified as follows:

- remove capacitors C24, C25
- remove IF transformer TR1
- connect IFOUTB to ground with the resistor R15 (0Ω)
- add a strap to connect the IF output to the SMA connector (see figure 93)
- change the resistor R26 to 27Ω.
-

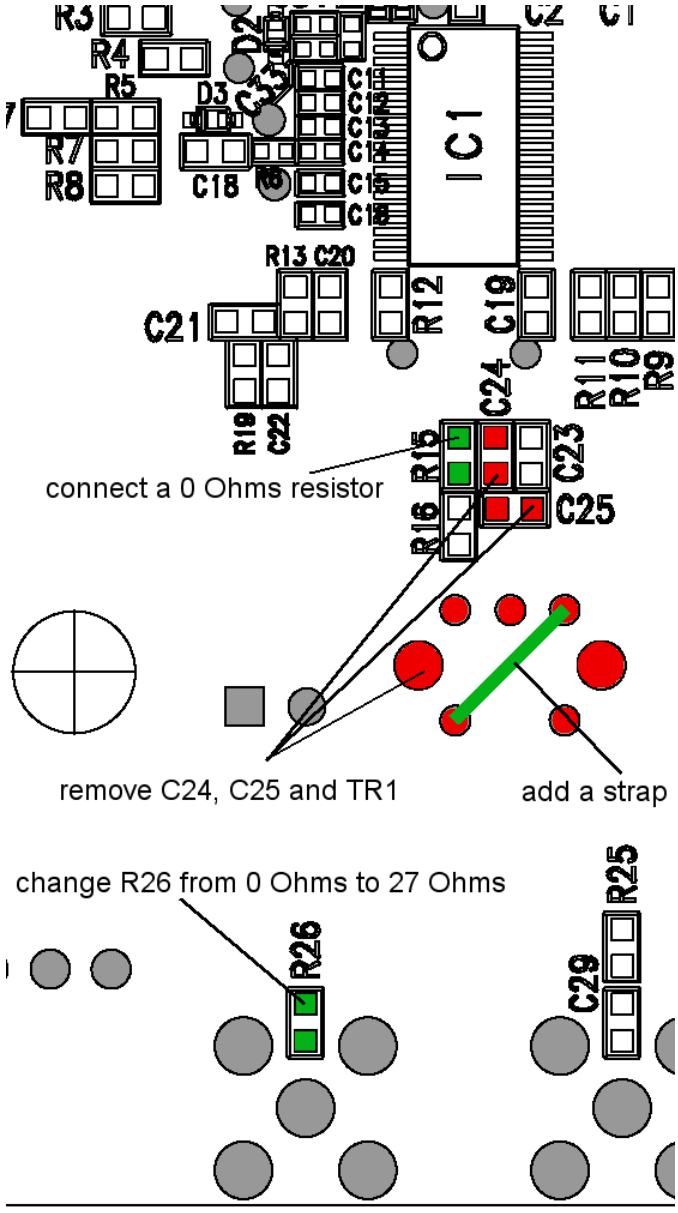


figure 93. Board modifications in asymmetrical mode.

9 CONCLUSION

The TDA6650/51TT benefits from the PHILIPS expertise in RF, both for mixer and oscillator design concepts. It also proposes a new architecture to fulfil the requirements of digital standards:

- The fractional-N architecture allows phase noise performance compatible with OFDM standards.
- The wide band AGC detector enables the handling of high adjacent channels.
- The switchable amplifier offers an easy to use solution to drive either symmetrical or asymmetrical load without any compromise on linearity.

This IC is fully dedicated to the reception of both analog and digital TV channels. Therefore, it can be used in digital and analog terrestrial tuners (OFDM, PAL…) and also in cable tuners (QAM).